Unit 2

Digital Circuits (Logic)

Unit Goals

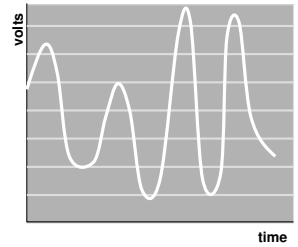
- Provide a high-level overview of digital hardware that will familiarize you with relevant concepts that will be explored throughout the course
- Topics of Importance:
  - Basic logic gates and their truth tables
  - Digital design metrics and goals
  - Single-variable Boolean algebra theorems
  - Combinational vs. sequential logic

Moving from voltages to 1's and 0's…

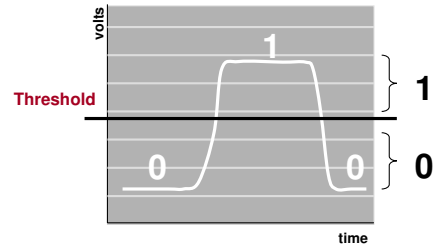
ANALOG VS. DIGITAL

Signal Types

- Analog signal
  - Continuous time signal where each voltage level has a unique meaning
  - Most information types are inherently analog
- Digital signal
  - Continuous signal where voltage levels are mapped into 2 ranges meaning 0 or 1
  - Possible to convert a single analog signal to a set of digital signals

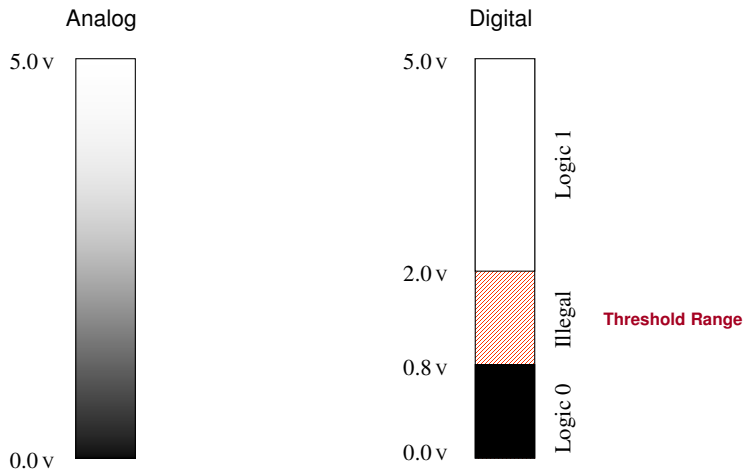


Analog



Digital

Signals and Meaning



Each voltage value has unique meaning

Each voltage maps to '0' or '1'
(There is a small illegal range where meaning is undefined since threshold can vary based on temperature, small variations in manufacturing, etc.)

Analog vs. Digital

USC students used to program analog computers!

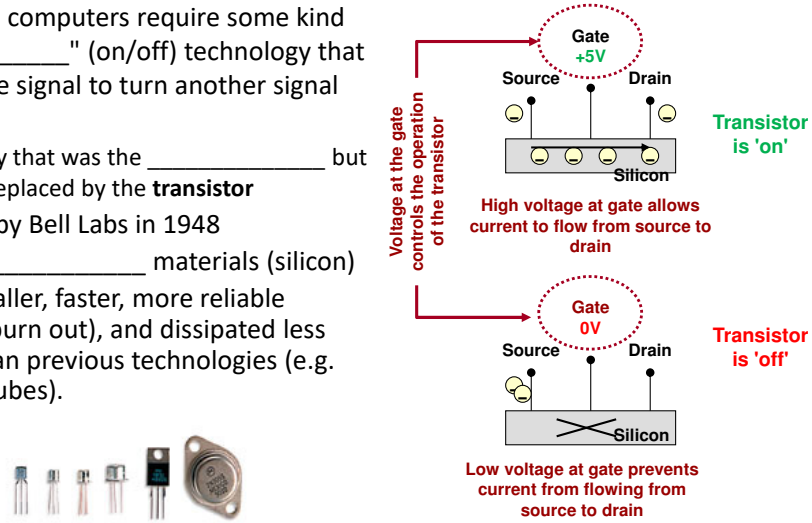
A Brief History

COMPUTERS, SWITCHING TECHNOLOGY, AND TRANSISTORS

You will not be tested on specifics of transistor operation, but should understand their fundamental role as the building blocks of logic circuits and their abstraction as a switch.

Transistor Overview

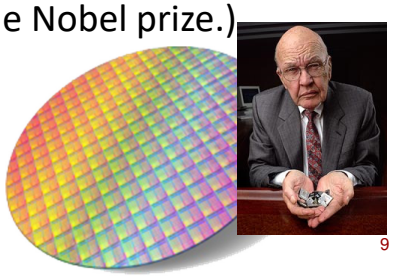
- Electronic computers require some kind of "_____" (on/off) technology that allows one signal to turn another signal on or off
  - Initially that was the _____ but then replaced by the **transistor**
- Invented by Bell Labs in 1948
- Uses _____ materials (silicon)
- Much smaller, faster, more reliable (doesn't burn out), and dissipated less power than previous technologies (e.g. vacuum tubes).



Individual Transistors
(About the size of your fingertip)

Little Things Can Change the World

- Electronic devices can be built from _____ transistors but would be extremely _____ to wire and assemble at any scale
- In 1958, Jack Kilby of Texas Instruments fabricates (and wires) multiple transistors on a single semiconductor substrate and the "_____ circuit" is born (and Kilby gets the Nobel prize.)



Moore's Law & Transistors

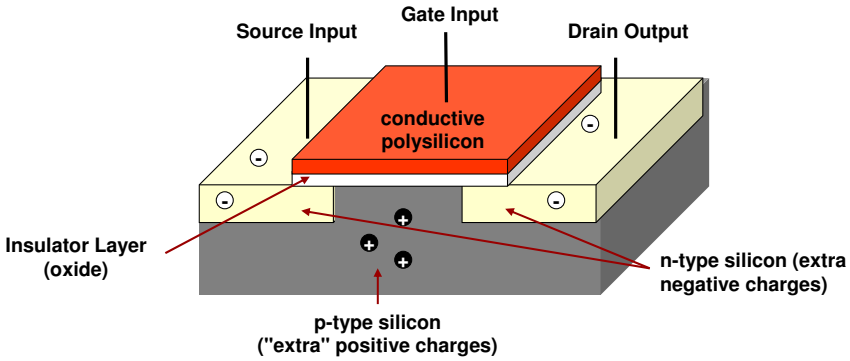
- We continue to shrink the size of the transistor structure
- Moore's Law = Number of transistors able to be fabricated on a chip will _____ _____
  - We are approaching the physical limitations of this shrinking
  - _____ compound annual growth rate over 50 years
    - No other technology has grown so fast so long
- Transistors are the fundamental building block of computer HW
  - Switching devices: Can conduct [on = 1] or not-conduct [off = 0] based on an input voltage

How Does a Transistor Work

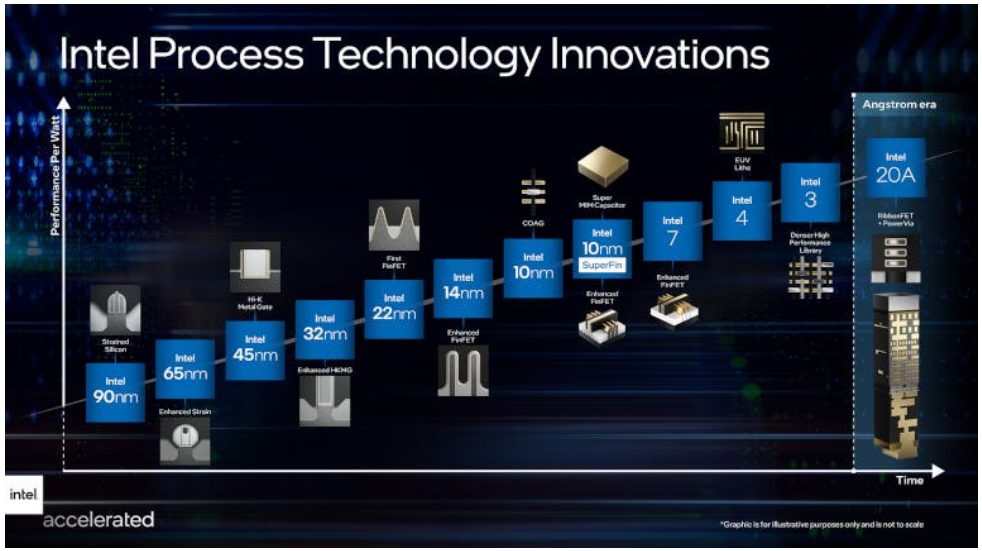
- Transistor inner workings
  - http://www.youtube.com/watch?v=IcrBqCFLHIY

NMOS Transistor Physics

- A thin, insulator layer (silicon dioxide or just "oxide") is placed over the silicon between source and drain
- Conductive polysilicon material is layered over the oxide to form the gate input

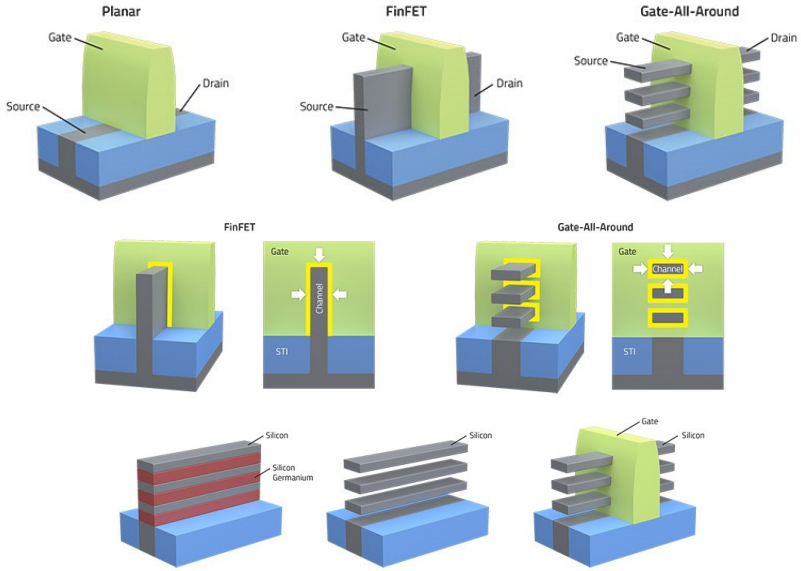


Minimum Feature Size



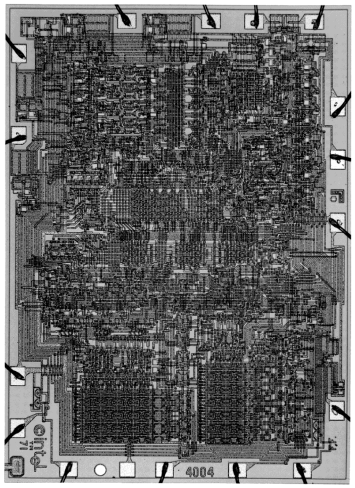
https://img.electronicdesign.com/files/base/ebm/electronicdesign/image/2021/08/Intel_Process_Roadmap_1_edit.610a0f6361e0d.png

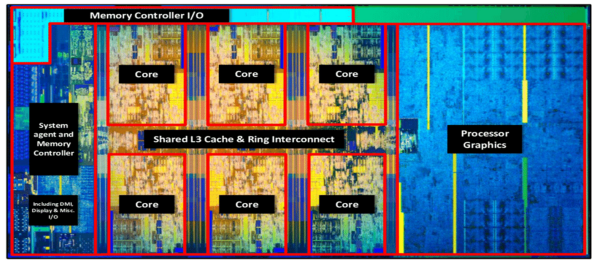
New Transistor Technologies



https://blog.lamresearch.com/finfets-give-way-to-gate-all-around/

Processor Trends





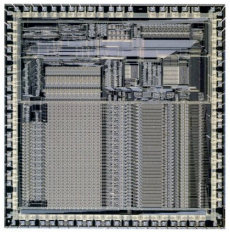
- 8th Gen Coffee-Lake Processor
- #cores/#threads: 6/12
- Technology node: 14nm wire width
- Clock speed: 3.7 GHz
- Transistor count: Over one billion
- Cache: 12MB

1971 – Intel 4004
1000 transistors
10,000 nm wire width
Max 4K-bits addressable memory
1 MHz operation

Apple's M1 (ARM based) Chip

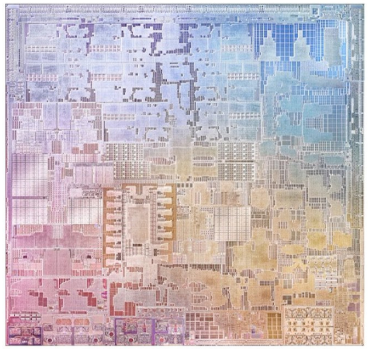
- 8 cores
- Technology node: 5 nm
- Up to 16 billion transistors
- Clock speed: ~3.2 GHz

ARM1 and Apple M1 at the same scale



ARM1 processor
~7mm wide
3 µm process

If built with M1 transistors, the entire ARM1 chip would be the tiny dot inside this circle: ∘

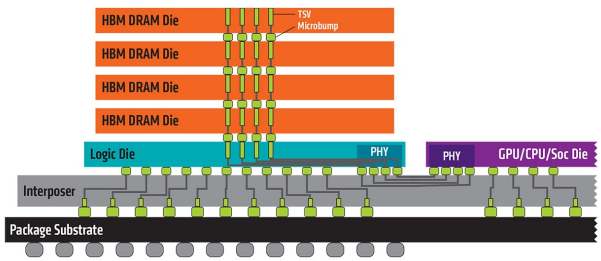


Apple M1 processor, ~11mm wide, 5 nm process

https://pbs.twimg.com/media/EmqIIIsVcAAUlm5.jpg

3D Chips

- Stacked chip dies in one package for memory or other processing accelerators rather than separate chips provide greater size, power, and speed advantages

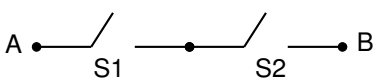


https://www.amd.com/en/technologies/hbm

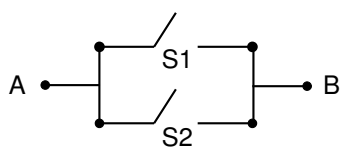
DIGITAL LOGIC GATES

Transistors and Logic

- Transistors act as switches (on or off)
- Logic operations (AND / OR) formed by connecting them in specific patterns
  - Series Connection
  - Parallel Connection



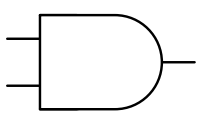
Series Connection
S1 **AND** S2 must be on for A to be connected to B



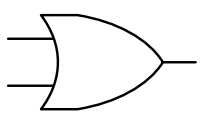
Parallel Connection
S1 **OR** S2 must be on for A to be connected to B

Gates

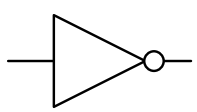
- Each logical operation (AND, OR, NOT) can be implemented as a digital device called a "gate"
  - The schematic symbols below are used to represent each logic gate
- Each logic gate can be built by connecting transistors in various configurations



AND Gate



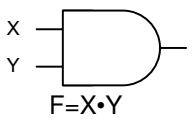
OR Gate



NOT Gate

AND Gates

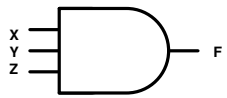
- An AND gate outputs a '1' (true) if ALL inputs are '1' (true)
- Gates can have several inputs
- Behavior can be shown in a truth table (listing all possible input combinations and the corresponding output)



F=X•Y

X	Y	F
0	0	0
0	1	0
1	0	0
1	1	1

2-input AND



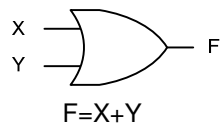
F=X•Y•Z

X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3-input AND

OR Gates

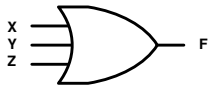
- An OR gate outputs a '1' (true) if ANY input is '1' (true)
- Gates can also have several inputs



F=X+Y

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	1

2-input OR



F=X+Y+Z

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

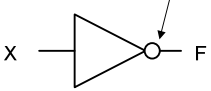
3-input OR

Buffer & NOT (Inverter) Gate

- A Buffer simply passes a digital value
  - But strengthens it _____ (e.g. boosts 3.7V closer to 5V)
- A NOT (aka "_____") gate inverts a digital signal to its opposite value (i.e. flips a bit)

X	F
0	0
1	1

F = X



the "bubble" (logically performs the inversion)

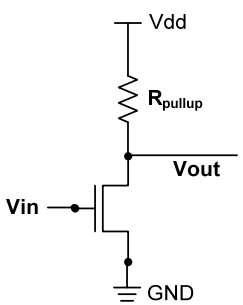
X	F
1	0
0	1

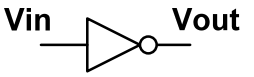
F = $\overline{X}$ or X'

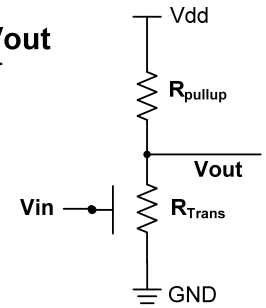
bar or ' mean inversion

Aside: How Do You Build an Inverter (1)?

- A simple (though maybe not ideal) method to build an inverter is to place a transistor in _____ with a resistor
  - Input to inverter is input to transistor
  - Output of inverter is node between resistor and transistor
- We can model the transistor as a _____
- Develop an equation for Vout using the voltage divider eqn.



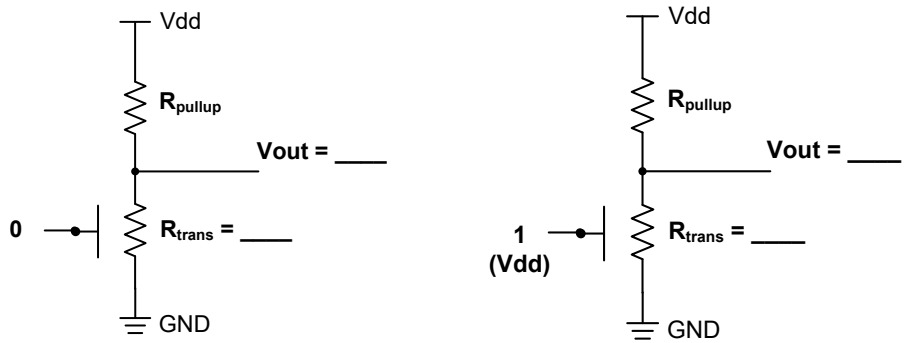




Vout = _____

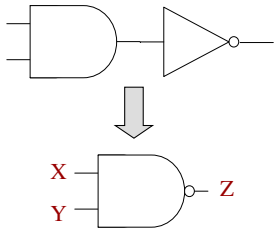
Aside: How Do You Build an Inverter (2)?

- First, estimate the resistance of R_{trans} if Vin is 0 (low) then again if Vin is 1 (high-voltage)
- Use that estimate in your equation for Vout to determine the output voltage



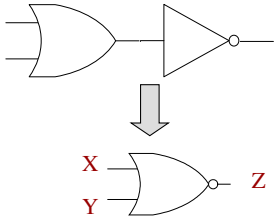
NAND and NOR Gates

- Inverted versions of the AND and OR gate



NAND

$$Z = \overline{X \cdot Y}$$



NOR

$$Z = \overline{X + Y}$$

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

NAND

True if NOT ALL inputs are true

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

OR

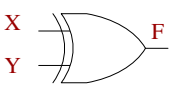
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

NOR

True if NOT ANY input is true

XOR and XNOR Gates

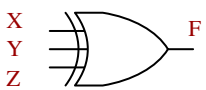
- Exclusive OR gate. Outputs a '1' if either input is a '1', but not both.



XOR

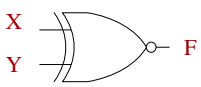
$$F = X \oplus Y$$

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	0



X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

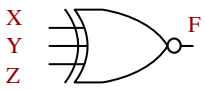
True if an odd # of inputs are true
= True if inputs are different



XNOR

$$F = \overline{X \oplus Y}$$

X	Y	F
0	0	1
0	1	0
1	0	0
1	1	1



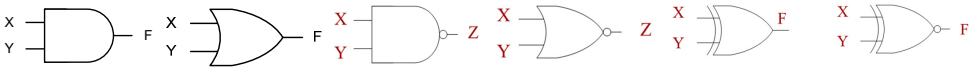
X	Y	Z	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

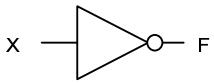
True if an even # of inputs are true
= True if inputs are same

Gate Summary

- You should know and memorize the truth tables of these basic gates

X	Y	AND	OR	NAND	NOR	XOR	XNOR
0	0	0	0	1	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	1	0	0	0	1

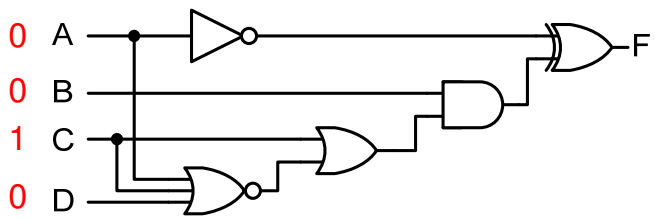




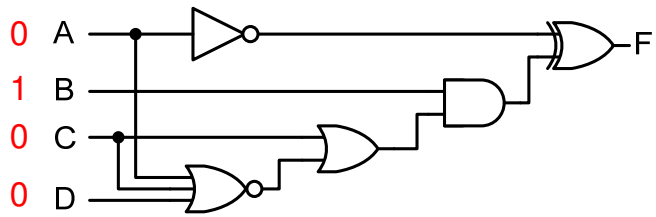
X	F
1	0
0	1

Logic Example

- To build useful digital circuits often requires networks of gates where one output feeds the input of another gate



Logic Example



Speed, area, and power

DIGITAL DESIGN GOALS

Digital Design Goals

- When designing a circuit, we want to optimize for the following three things:
  - _____ (minimize)
  - _____ (maximize) or _____ (minimize)
  - _____ (minimize)
- Can usually only optimize _____
  - There is a huge trade space! This is what engineering is all about!

Minimizing Circuit Area

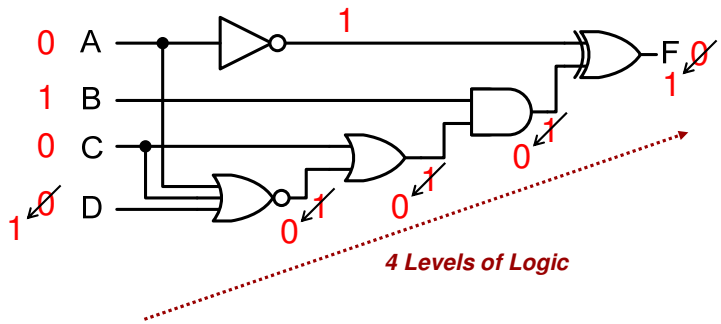
- Approaches:
  - Reduce the _____ used to implement a circuit
  - Reduce the number of _____ to each gate
    - In general a gate with n inputs requires ____ transistors to implement
- Simplify logic expressions (usually by factoring and then canceling terms) to reduce the number of gates
  - We'll learn more about this soon

Maximizing Speed

- Speed is affected by:
  - _____ (path length)
  - _____
  - Number of inputs (fan-in) to the gate
    - Usually limited to _____ input gates
  - Number of outputs a gate connects to (fan-out)
  - Feature size and implementation technology

Delay Example

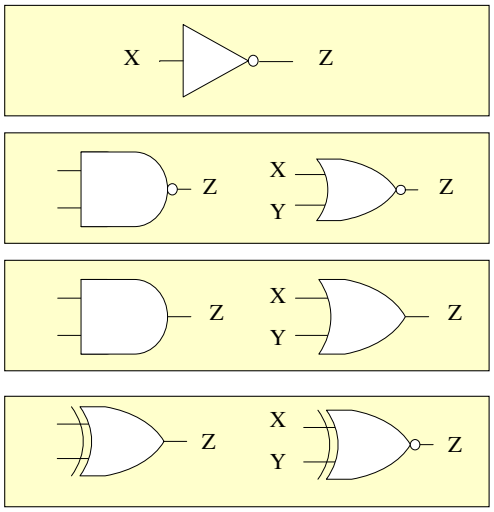
- Gates take time for the output to change once the inputs change (aka propagation delay)
- Levels of Logic = _____ # of gates on _____ from input to output



Change in D, C, or A must propagate through 4 levels of gates

Gate Delays

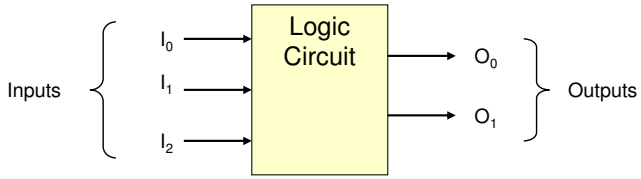
- Order the gate types in terms of fastest to slowest?
- Typical gate delay for a 2-input NAND or NOR is under a 100 ps.



Logical Operations Summary

- All digital circuits can be described using AND, OR, and NOT
  - Note: You'll learn in future courses that digital circuits can be described with any of the following sets:
    - {AND, NOT}, {OR, NOT}, {NAND only}, or {NOR only}
- Normal convention: 1 = true / 0 = false
- A logic circuit takes some digital inputs and transforms each possible input combination to a desired output values

Trivia-of-the-day: The Apollo Guidance Computer that controlled the lunar spacecraft in 1969 was built out of 8,400 3-input NOR gates.



BOOLEAN ALGEBRA INTRO

Boolean Algebra Intro

- Larger logic circuits are too complex to analyze with truth tables or schematics
- Instead, describe the action of the circuit by a mathematical equation using Boolean algebra. Use axioms and theorems to help us manipulate, and perhaps simplify, the equation
  - Axioms = Basis / assumptions used
    - Digital signals / _____ variables: Only _____
    - __ fundamental logic operations: _____
  - Theorems = Statements derived from axioms

Single Variable Theorems

- Provide some simplifications for expressions containing:
  - a single variable
  - a single variable and a constant bit
- Each theorem has a dual (another true statement)
  - Dual is formed by swapping ___ <=> ___ as well as _____ <=> _____
- Each theorem can be proved by writing a truth table for both sides (i.e. proving the theorem holds for all possible values of X)

T1	**X + 0 = X**	**T1'**	**X • 1 = X**
T2	**X + 1 = 1**	**T2'**	**X • 0 = 0**
T3	**X + X = X**	**T3'**	**X • X = X**
T4	**(X')' = X**		
T5	**X + X' = 1**	**T5'**	**X • X' = 0**

Duality

- The "dual" of an expression is not equal to the original

$$\underset{\text{Original expression}}{1+0} \neq \underset{\text{Dual}}{0 \bullet 1}$$

- Taking the "dual" of both sides of an equation yields a new equation

$$\underset{\text{Original equation}}{X+1=1} \Rightarrow \underset{\text{Dual}}{X \bullet 0 = 0}$$

- Boolean algebra theorems are LOGO (learn-one, get one free)

Single Variable Theorem (T1)

X+0 = X (T1)

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

OR

Hold Y constant

X•1 = X (T1')

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND

Whenever a variable is OR'ed with 0, the output will be the same as the variable…

"0 OR Anything equals that _____"

Whenever a variable is AND'ed with 1, the output will be the same as the variable…

"1 AND Anything equals that _____"

Single Variable Theorem (T2)

X+1 = 1 (T2)

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

OR

Hold Y constant

X•0 = 0 (T2')

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND

Whenever a variable is OR'ed with 1, the output will be 1…

"1 OR anything equals _____"

Whenever a variable is AND'ed with 0, the output will be 0…

"0 AND anything equals _____"

Single Variable Theorem (T3)

X+X = X (T3)

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

OR

X•X = X (T3')

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND

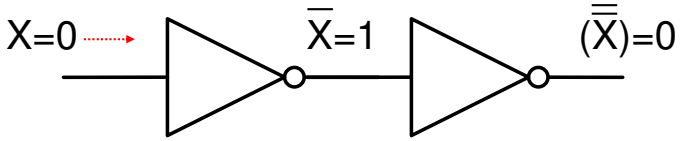
Whenever a variable is OR'ed with itself, the result is just the value of the variable

Whenever a variable is AND'ed with itself, the result is just the value of the variable

This theorem can be used to reduce two identical terms into one *OR* to replicate one term into two.

Single Variable Theorem (T4)

$$(\overline{\overline{X}}) = X \text{ (T4)}$$



X	$\overline{X}$	$\overline{\overline{X}}$
1	0	1
0	1	0

Anything inverted twice yields its original value

Single Variable Theorem (T5)

$$X+\overline{X} = 1 \text{ (T5)} \qquad X \bullet \overline{X} = 0 \text{ (T5')}$$

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

OR

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND

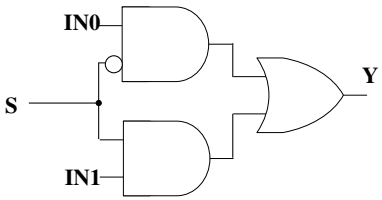
Whenever a variable is OR'ed with its complement, one value has to be 1 and thus the result is 1

Whenever a variable is AND'ed with its complement, one value has to be 0 and thus the result is 0

This theorem can be used to simplify variables into a constant or to expand a constant into a variable.

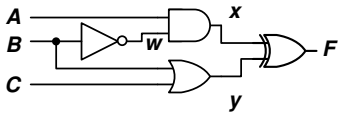
Practice

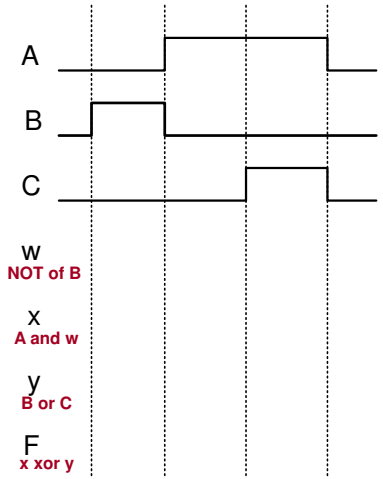
- **Exercise 1**: Given the circuit below, write the corresponding logic equation for Y
- **Exercise 2**: Suppose we learn S=0, simply the equation for Y using T1-T5
- **Exercise 3**: Suppose we learn S=1, simply the equation for Y using T1-T5



Practice: Waveform Diagrams

- Waveform diagrams show digital circuit operation over time
  - Vertical axis: Each signal can be HIGH (1) or LOW (0)
  - Horizontal axis: time
- Complete the waveform for the given circuit using T1 and T2 to speed your work





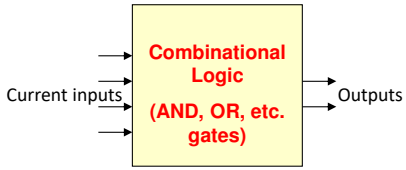
Processing and Storing bits

COMBINATIONAL VS. SEQUENTIAL LOGIC

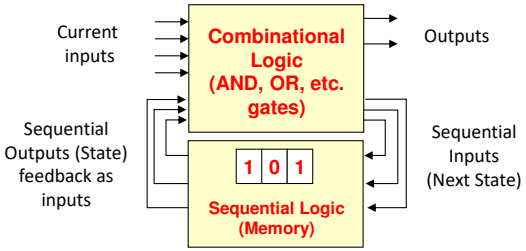
Combinational vs. Sequential Logic

- All logic is categorized into 2 groups
  - Combinational logic:
    - Outputs = f(_____)
    - _____ circuits – Outputs only depend on inputs now
  - Sequential Logic
    - Outputs = f(_____)
    - **Stateful** (having "_____" **or storage**) - Remembering inputs or events that happened in the past

Combinational vs. Sequential



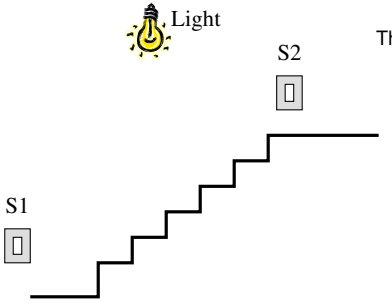
Outputs depend only on current inputs



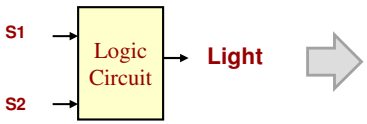
Outputs depend on current inputs and previous inputs (previous inputs summarized via state)

Combinational Example: Staircase Light Switch

Whether or not the light is on is only dependent on the current position of the switches



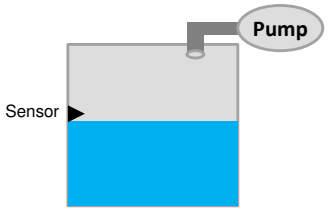
The light, **L**, should be on when…

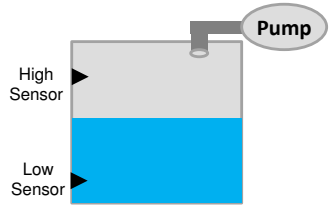


S1	S2	Light
0	0	
0	1	
1	0	
1	1	

Water Tank Problem

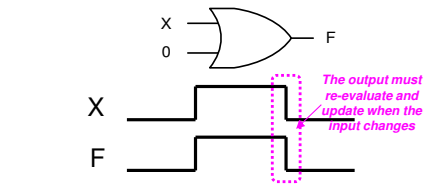
- Build a control system for a pump to keep the tank from going empty



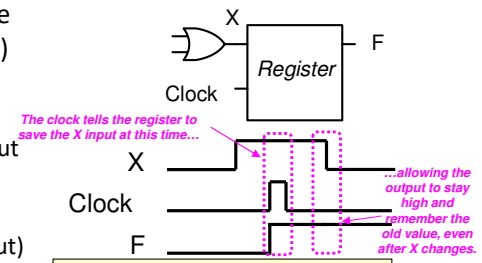


Sequential Devices (Registers)

- AND, OR, NOT, NAND, and other gates are ***combinational logic***
  - Outputs only depend on what the inputs are **right now**, not one second ago
  - Cannot _____ what happened previously
- ***Sequential logic*** devices such as a "_____" can save or **remember** a value (even after the input is changed/removed)
  - Usually have a controlling signal (aka the "**clock**") that indicates when the device should "**sample and hold**" the current input
  - Analogy: Taking a _____ with your phone…when you press a button (clock pulse) the camera samples the scene (input) and _____ it as a snapshot (output).



With combinational circuits, the output must be generated based only on the current inputs.



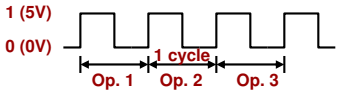
With sequential logic, the output can be based on past inputs and thus the output may be remembered even after the input changes.

Pulses and Clock Period

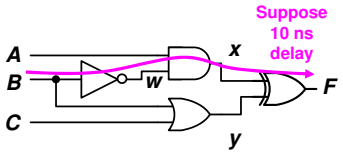
- Registers (flip-flops) need a clock pulse edge to trigger
- We can generate pulses at _____ times that we know the data we want has arrived (at some irregular interval)
- Other registers in our hardware should trigger at a _____ interval (i.e. period, **T**)
  - Alternating _____ voltage pulse train
  - 1 cycle is usually measured from rising/positive edge to rising/positive edge
  - Clock frequency (**F**) = # of cycles per second
  - **F =** _____
- The clock period of a digital circuit is set based on the _____ delay path from the _____ of a register to the _____ of the next

Aperiodic (Irregular) Clock Pulses

Periodic (Regular) Clock Signal



2 GHz = $2*10^9$ cycles per second = 0.5 ns/cycle



Clock Period (T) must be > 10 ns (i.e. F < 100 MHz)

Summary

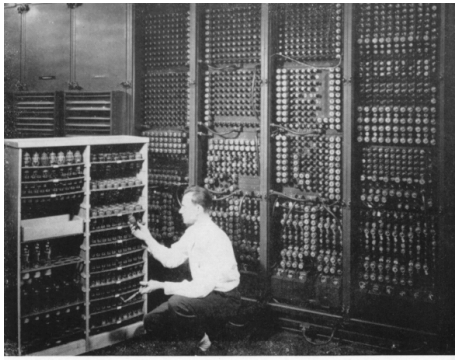
- Combinational logic corresponds to _____ that manipulate number (similar to software operators +, -, *, /, <, >, etc.)
- Sequential logic corresponds to _____ that can store values for further processing

A Brief History

COMPUTERS AND SWITCHING TECHNOLOGY

Electronic Computers

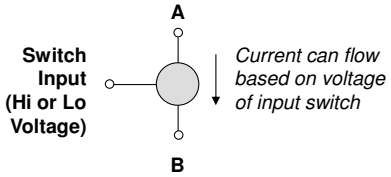
- Replaced mechanical computation engines
- Electronic computers require some kind of _____ (on/off) technology
  - Initially that was the _____
- Example: ENIAC (1945)
  - One of the first, fully electronic computers
  - Used _____ vacuum tubes
  - Weighed 30 tons
  - _____ square feet
  - Largest number range: 10 decimal digits (±9,999,999,999)
- Many early computers were programmed with patch panels (wire plugs)



Replacing a bad tube meant checking among ENIAC's 19,000 possibilities.

Vacuum Tube Technology

- Digital, electronic computers use some sort of voltage controlled switch (on/off)
- Looks like a light bulb
- Usually 3 nodes
  - 1 node serves as the switch value allowing current to flow between the other 2 nodes (on) or preventing current flow between the other 2 nodes (off)
  - Example: if the switch input voltage is 5V, then current is allowed to flow between the other nodes



Vacuum Tube

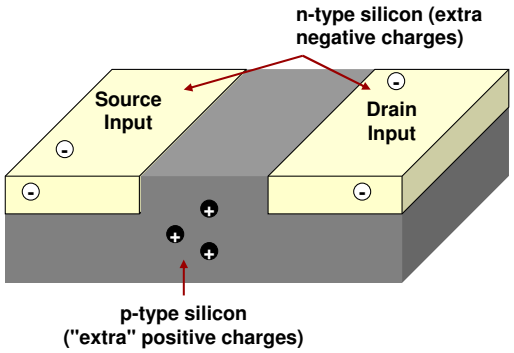
Vacuum Tube Disadvantages

- _____
  - Especially when you need _____ _____
- _____
  - Can _____
- _____

UNUSED

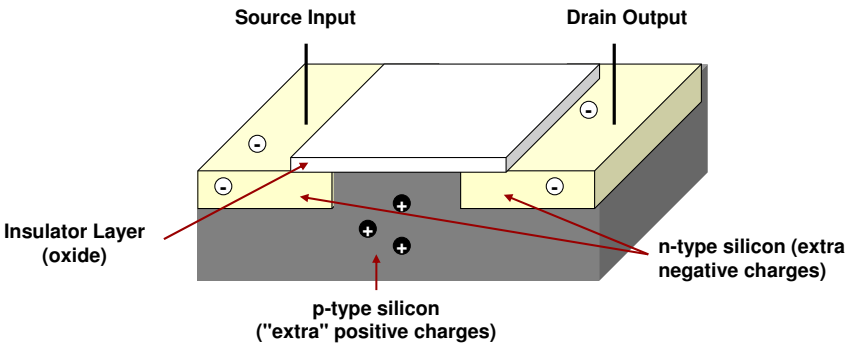
NMOS Transistor Physics

- Let's review what we saw in the video…
- Transistor is started by implanting two n-type silicon areas, separated by p-type



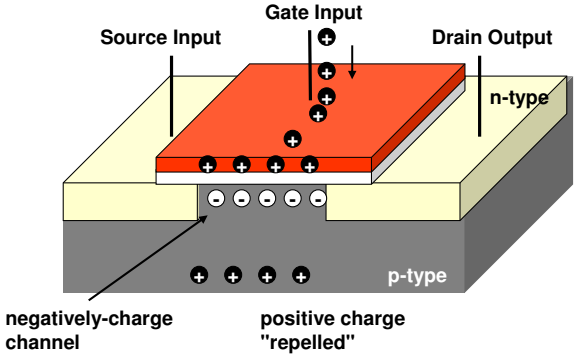
NMOS Transistor Physics

- A thin, insulator layer (silicon dioxide or just "oxide") is placed over the silicon between source and drain



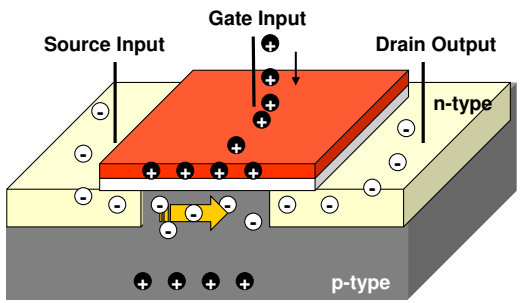
NMOS Transistor Physics

- Positive voltage (charge) at the gate input *repels* the extra positive charges in the p-type silicon
- Result is a negative-charge channel between the source input and drain



NMOS Transistor Physics

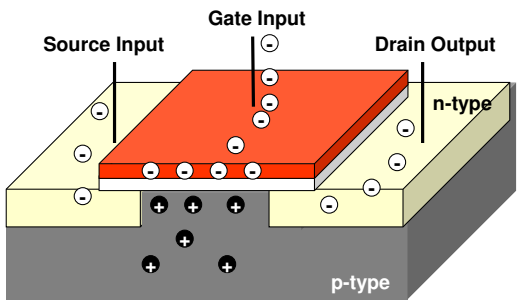
- Electrons can flow through the negative channel from the source input to the drain output
- The transistor is "on"



Negative channel between source and drain = Current flow

NMOS Transistor Physics

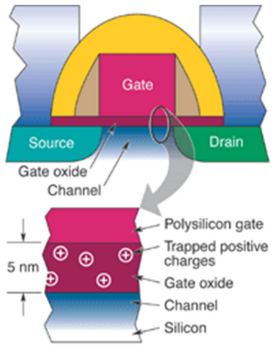
- If a low voltage (negative charge) is placed on the gate, no channel will develop and no current will flow
- The transistor is "off"

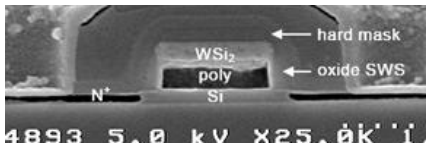


No negative channel between source and drain = No current flow

View of a Transistor

- Cross-section of transistors on an IC
- Moore's Law is founded on our ability to keep shrinking transistor sizes
  - Gate/channel width shrinks
  - Gate oxide shrinks
- Transistor feature size is referred to as the implementation "technology node"

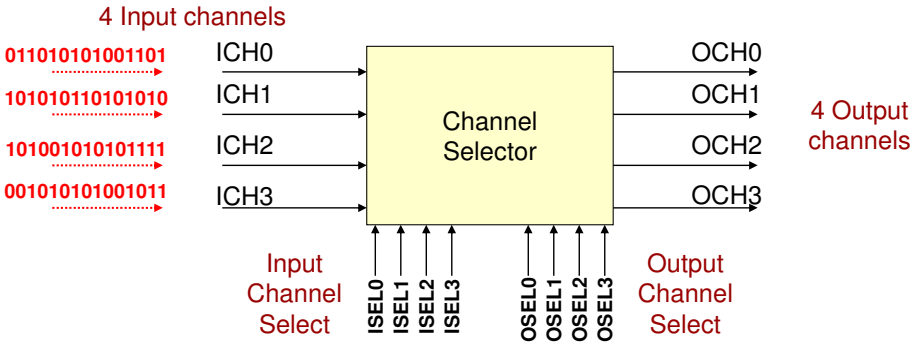




Electron Microscope View of Transistor Cross-Section

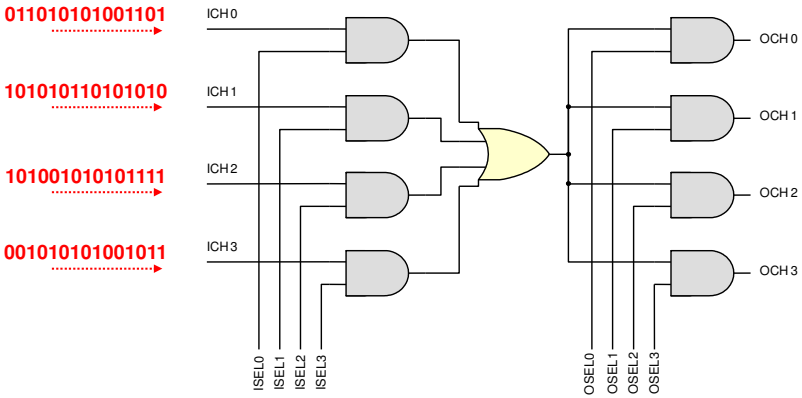
Application (if time): Channel Selector

- Given 4 input, digital music/sound channels and 4 output channels
- Given individual "select" inputs that select 1 input channel to be routed to 1 output channel



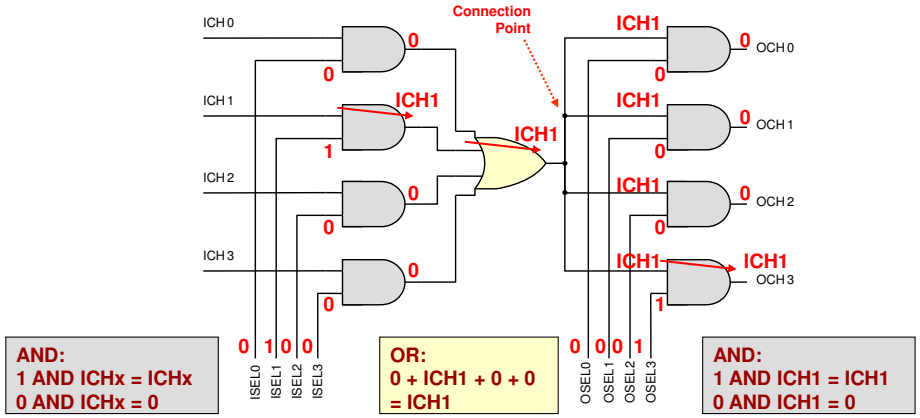
Application: Steering Logic

- 4-input music channels (ICHx)
  - Select one input channel (use ISELx inputs)
  - Route to one output channel (use OSELx inputs)



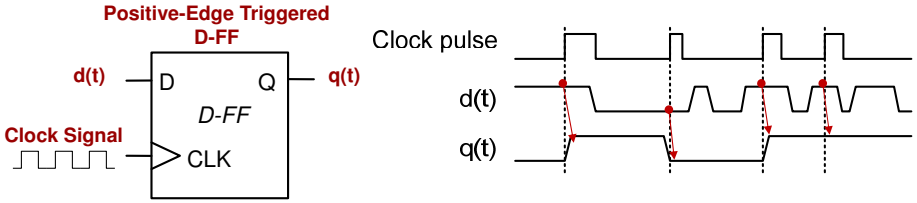
Application: Steering Logic

- 1st Level of AND gates act as barriers only passing 1 channel
- OR gates combines 3 streams of 0's with the 1 channel that got passed (i.e. ICH1)
- 2nd Level of AND gates passes the channel to only the selected output



Flip-Flops

- Devices called flip-flops are the building blocks of _____
  - 1 Flip-flop PER bit of input/output (i.e. a 4-bit register => ___ flip-flops)
  - There are many kinds of flip-flops but the most common is the D- (Data) Flip-flop (a.k.a. D-FF)
- D Flip-flops save the value on their D input whenever the clock _____ from 0 -> 1 (i.e. on the clock edge) and output that saved value of D on the Q output until the next edge
  - _____: instant the clock transition from low to high (0 to 1)



Usage of Sequential Logic

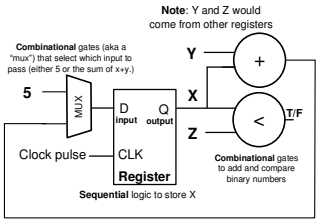
- Sequential logic (i.e. registers) is used to store values
  - Each register is analogous to a _____ in your software program
  - Remembers a value until told to update
- Combinational logic is used to _____ bits (i.e. perform _____ on values
  - Analogous to operators (+,-,*) in your software program

```
int x = 5;
...

x = x + y;

// x's value
// remembered for
// later use
if(x > z)
{

}
```



Pulses and Clock Period

- Registers need a clock pulse edge to trigger
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- Other registers in our hardware should trigger at a _____ interval (i.e. period, **T**)
  - Alternating _____ voltage pulse train
  - 1 cycle is usually measured from rising/positive edge to rising/positive edge
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  - **F = _____**
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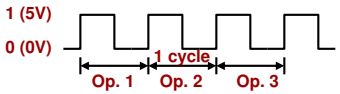
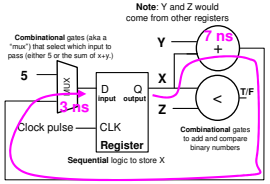
Aperiodic (Irregular) Clock Pulses

Periodic (Regular) Clock Signal



2 GHz = $2*10^9$ cycles per second = 0.5 ns/cycle



Clock Period (T) must be > 10 ns (i.e. < 100 MHz)