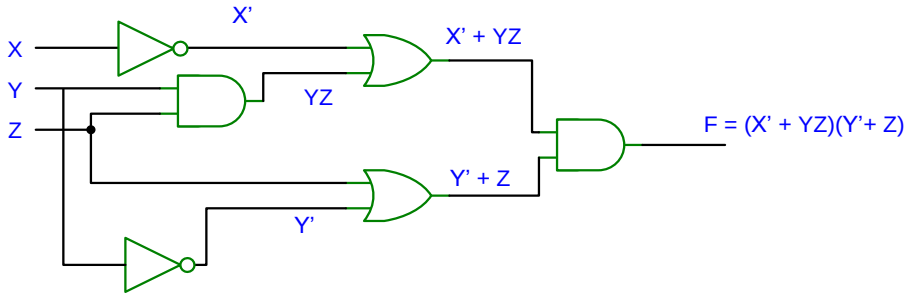
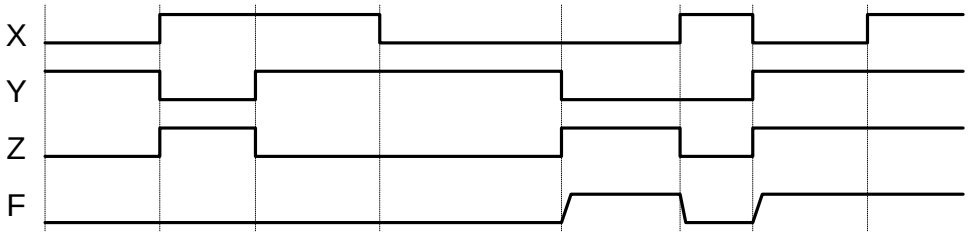
EE 109 Homework 4

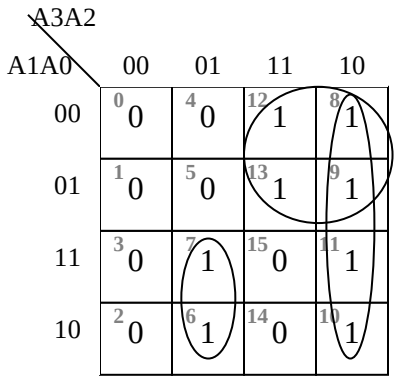
Name: ___Solutions_____
Due: **Score: _____**
Show work to get full credit. Remember, use on only one side of the paper and staple them

1.



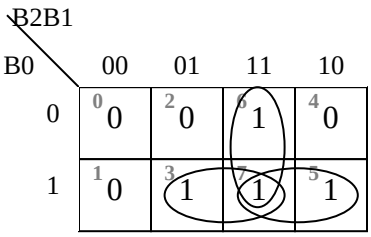


2. a

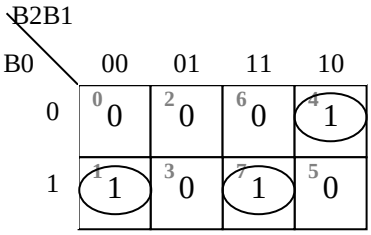


F = A3'A2A1 + A3A2' + A3A1'

b.



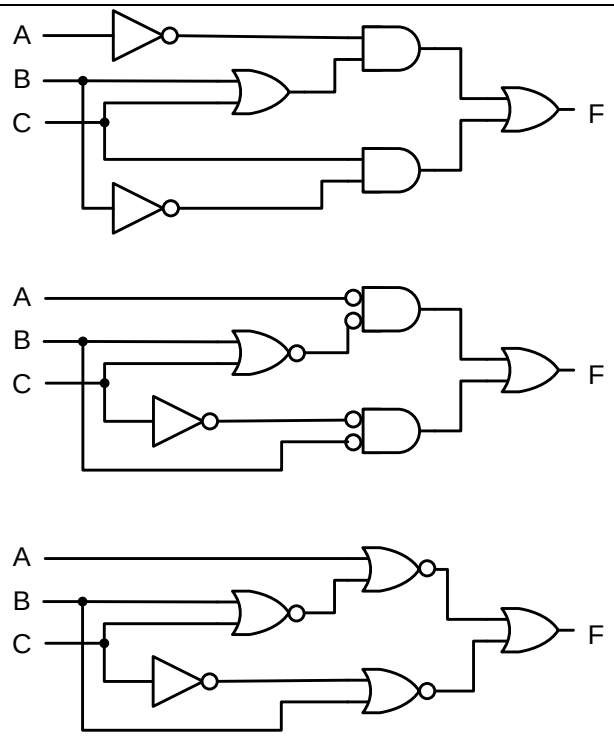
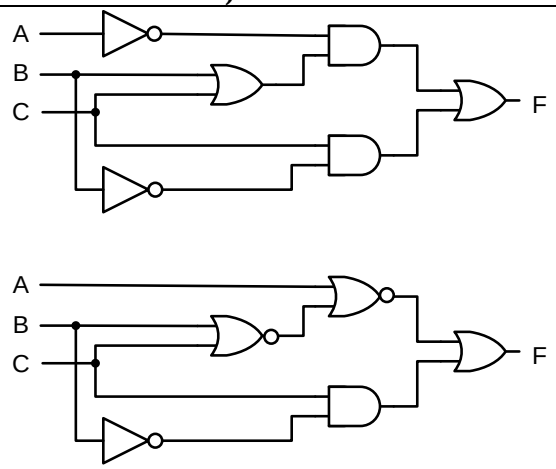
G1 = B2B1+B2B0+B1B0



G0 = B2'B1'B0 + B2B1'B0'+B2B1B0

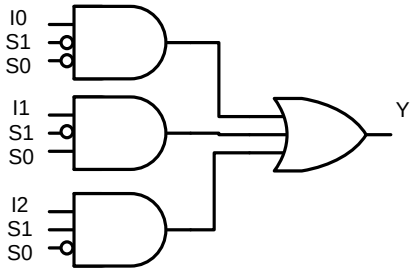
3. **Original -> Manipulating inverters -> Final circuit**

Both Solutions are Acceptable and should receive full credit

Solution 1 **(Rearrange = Move from one branch to another)**	**Solution 2** **(Rearrange = Not able to move from one branch to another)**
	

4. **[Paper]** (10 pts.) Draw a gate-level schematic of a 3-to-1 mux [Inputs: I0, I1, I2, and select bits S1,S0 and output Y] with the following function table:

S1	**S0**	**Y**
0	0	I0
0	1	I1
1	0	I2
1	1	unused

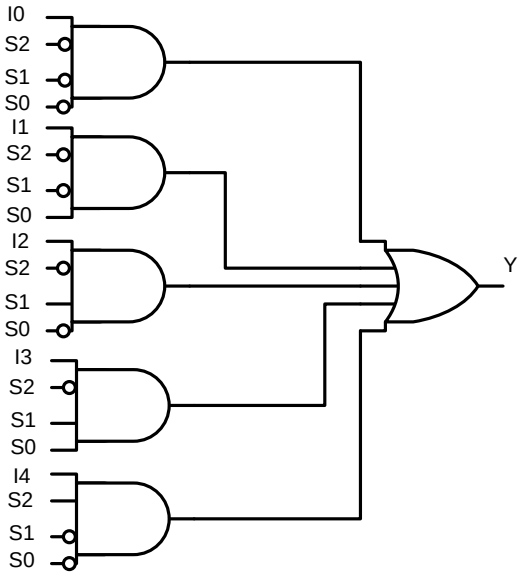


S0' optional

Note: The bottom AND gate can leave off S0-bar as an input because select case 11 is unused.

5. **[Paper]** (10 pts.) Draw a gate-level schematic of a 5-to-1 mux [Inputs: I0, I1, I2, I3, I4 and select bits S2,S1,S0 and output Y] with the following function table:

S2	S1	S0	Y
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4

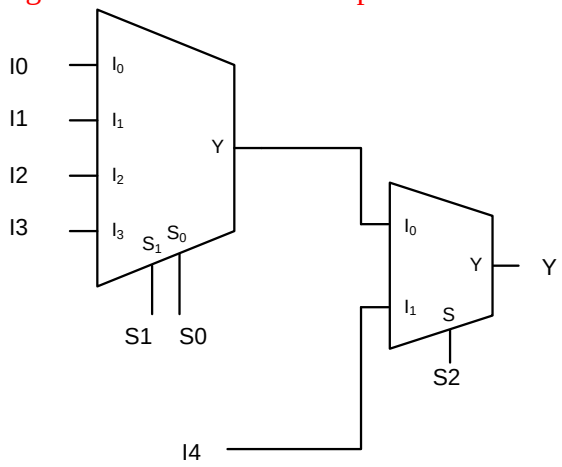


S1' & S0' optional

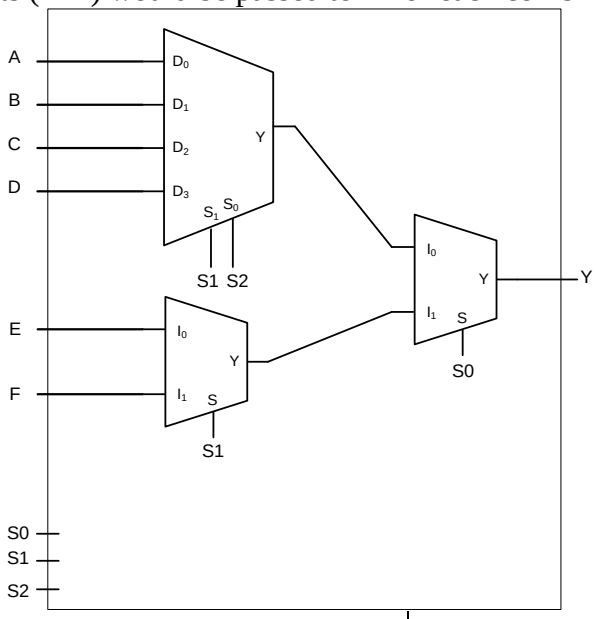
Note: The bottom AND gate can leave off S1-bar and S0-bar as an input because select case 1x1 and 11x are unused.

6. **[Paper]** Could you design the same 5-to-1 mux if we provided a single 4-to-1 mux and a single 2-to-1 mux. If so, show your design.

Yes (Note: I0 and I4 can be swapped **if and only if** the I0 goes to input 0 of the last-stage 2-to-1 mux and the output of the 4-to-1 mux connects to input 1 of the 2-to-1 mux.)



7. **[Paper] (10 pts.)** Examine the mux diagram below and complete the truth table by identifying what inputs (A-F) would be passed to Y for each combination of select bits.



S2	S1	S0	Y
0	0	0	A
0	0	1	E
0	1	0	C
0	1	1	F
1	0	0	B
1	0	1	E
1	1	0	D
1	1	1	F

8. **[Paper]** Suppose we change the select bit correspondence of the 5-to-1 mux from the previous problem to now be as shown in the table below. Could you design a 5-to-1 mux with a single 4-to-1 mux and single 2-to-1 mux. If so, show your design.

S2	S1	S0	Y
0	0	0	I0
0	1	0	I1
0	1	1	I2
1	0	0	I3
1	1	0	I4

Yes