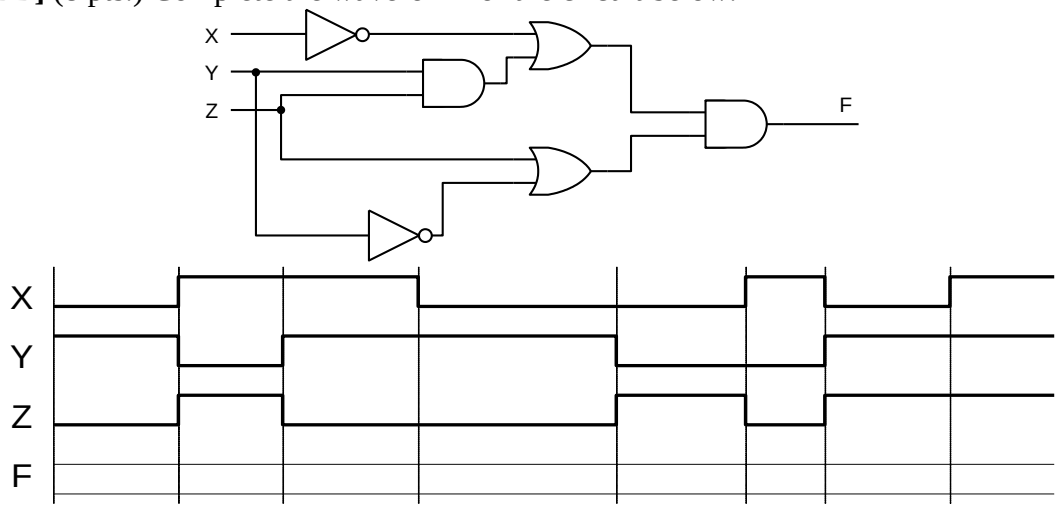
EE 109 Homework 4
Logic Function Synthesis and Muxes

Name: _____
Due: See Blackboard **Score:_____**

HW 4a Blackboard Form

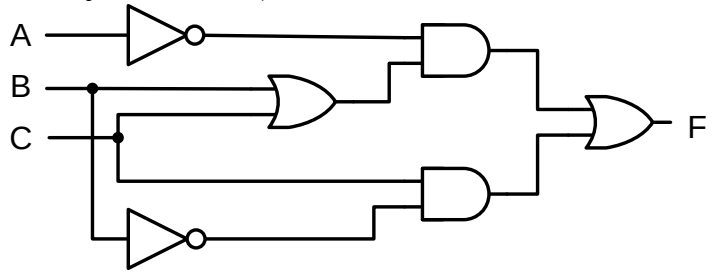
1. **[BB]** (8 pts.) Complete the waveform for the circuit below.



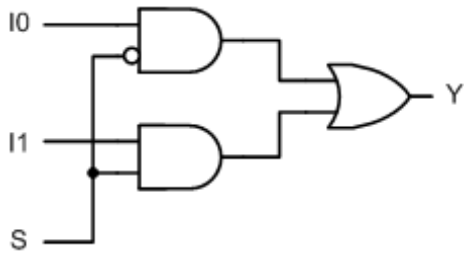
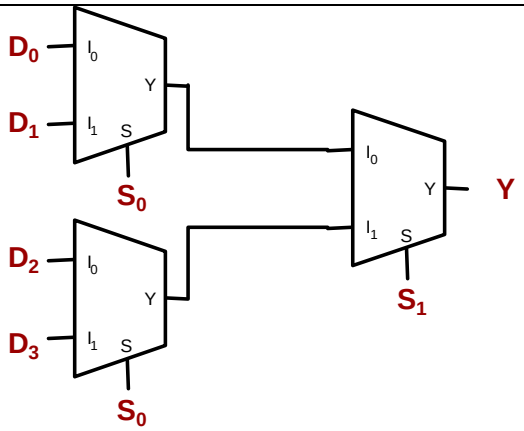
2. **[BB] (32 pts.) Using a Karnaugh map, find the minimal SOP expression for the described function.**
   a. A circuit that takes a 4-bit unsigned input A3,A2,A1,A0 and outputs a single value, F, true when the number is in the range 6 <= A[3:0] <= 13
   b. A circuit that takes a 3-bit unsigned input B[2:0] and outputs a 2-bit unsigned number, G[1:0] where the decimal value of G = B/3 + B%2 (assuming integer division)

HW 4b – Submit an Electronic Drawing / Scanned Picture of your Solutions on Gradescope

3. **[GS] (10 pts.)** By rearranging or removing (but not adding) inverters at the INPUTS, use DeMorgan's theorem to convert as many AND/OR gates as possible to NOR gates while ensuring the circuit implements the same function, F, as the original (i.e. is equivalent to the original). Redraw the equivalent circuit. **Note: Replacing an AND or OR with a NOR does not count as adding an inverter since a NOR gate is an indivisible gate (and not an OR followed by an inverter).**



Note: For the following questions, we will ask for a gate level schematic or a block diagram schematic. For block diagrams, please show both the external signals for the overall circuit being designed (a.k.a. "system" labels) and also label each input and output of each component (i.e. "device" labels).

	
A gate-level schematic shows the actual logic gates needed to implement the design and labels each input and output.	**A block diagram** shows boxes representing certain components and labels both the actual, external ("system") signals as well as which input/output is which for each component (i.e. "device labels" like I0, I1 within each block diagram)

4. **[GS] (10 pts.)** Draw a **gate-level** schematic of a 3-to-1 mux [Inputs: I0, I1, I2, and select bits S1,S0 and output Y] with the following function table:

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	Unused

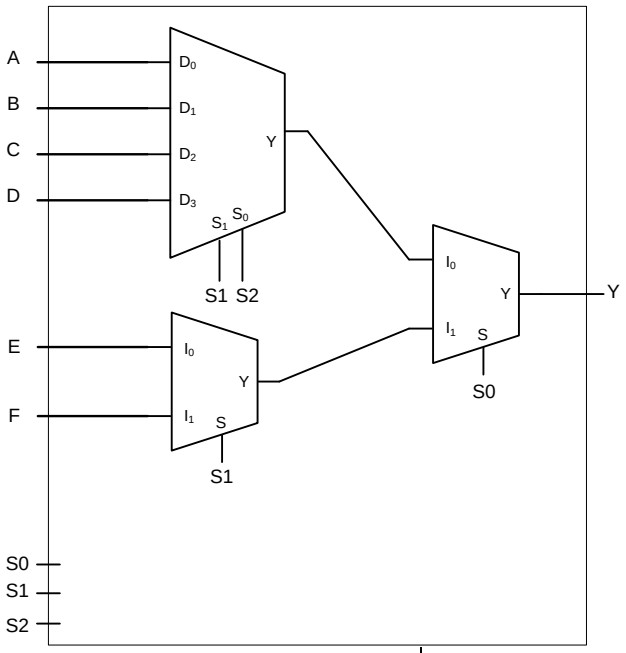
5. **[GS] (10 pts.)** Draw a **gate-level** schematic of a 5-to-1 mux [Inputs: I0, I1, I2, I3, I4 and select bits S2,S1,S0 and output Y] with the following function table:

S2	S1	S0	Y
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
	others		unused

Continue to next page

6. **[GS] (10 pts.)** Could you design the same 5-to-1 mux if we provided a single 4-to-1 mux and a single 2-to-1 mux. If so, show your design as a **block diagram** labeling the inputs of individual blocks and the overall mux.

7. **[GS] (10 pts.)** Examine the mux diagram below and complete the truth table by identifying what inputs (A-F) would be passed to Y for each combination of select bits.



S2	S1	S0	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

8. **[GS] (10 pts.)** Suppose we change the select bit correspondence of the 5-to-1 mux from the Q6 to now be as shown in the table below. Could you design a 5-to-1 mux with a single 4-to-1 mux and single 2-to-1 mux. If so, show your design as a **block diagram** labeling the inputs of individual blocks and the overall mux.

S2	S1	S0	Y
0	0	0	I0
0	1	0	I1
0	1	1	I2
1	0	0	I3
1	1	0	I4
others			unused