EE 109 Homework 3
Minterms/Maxterm/K-Maps

Name: _____

Due: See Website **Score: _____**

Please post any questions regarding HW problems on Piazza.

HW 3a Blackboard Form – Answer on Blackboard

1. **[BB] (16 pts.)** Derive the truth table for the following functions [One basic approach is to simply plug in each combination and evaluate the expression]. (Note: ' means NOT and unless there is parentheses around an expression the ' only applies to the single variable to its left).
   a. F = (A'+B')(C)
   b. G = WX' + XY' + W'

2. **[BB] (7 pts.)** Implement the following functions

	Color Bit Combinations		
Meaning	**C2**	**C1**	**C0**
Red	0	0	0
Orange	0	0	1
Yellow	0	1	0
Green	0	1	1
Blue	1	0	0
Indigo	1	0	1
Violet	1	1	0
Unused	1	1	1

   a. Build appropriate single gate (+ inverters) checker/decoders that outputs a logic '1' for each of the three primary colors: **Red, Blue, Yellow** (i.e. one decoder to check for each color)

   b. Build an appropriate single gate (+inverters) checker/decoder that outputs a logic '0' for each color: **Green, Blue, Indigo, Violet**.

3. **[BB] (6 pts.)** Given a child's age [0-7 years old], design logic to produce the following outputs: {**Baby, Toddler, Preschool, Kinder, Grade1, Grade2**} which have the following age correspondence/mapping. Use only 1 AND gate (and any number of inverters) per output.

	Age Combinations		
Meaning	**A2**	**A1**	**A0**
Baby	0	0	0
	0	0	1
Toddler	0	1	0
	0	1	1
Preschool	1	0	0
Kindergarten	1	0	1
Grade1	1	1	0
Grade2	1	1	1

4. **[BB] (5 pts.)** Given a 4-bit, unsigned input (A[3:0]) design a logic function, H, using a sum of minterms approach which outputs '1' if the input number is a multiple of 3 (i.e. A[3:0] is in the set $\{0_{10}, 3_{10}, 6_{10}, \ldots\}$. Write out the algebraic (equation using ANDs, ORs, and NOTs) form of the minterm representation for H (do not simplify).

5. **[BB] (5 pts)** Write out the algebraic (equation using ANDs, ORs, and NOTs) form of the sum of minterms representation for G (do not simplify…just keep the minterms as is).

   $G = \Sigma_{A,B,C,D}(2,3,6,13,15)$

6. **[BB] (5 pts.)** Now simplify the result you found from the previous problem to a minimal SOP expression.

7. **[BB] (6 pts.)** Use the theorems of Boolean algebra to find the minimal expression in the indicated form for each of the following logic functions:
   a. **Convert to minimal POS**: F = X+[(W'Y'Z)(W+(X'(Y+Z)))]
   b. **Convert to minimal SOP:**

$$G = \overline{(w + x + \bar{y})} + w\bar{x}y + (w\bar{z} + x\bar{y}) \cdot \overline{(x(\overline{w} + z))}$$

HW 3b – Submit on BB

8. **[Practice Only…Do not submit] Using only 2-input NOR gates (as many as you like for each part), build a circuit that is equivalent to the following circuits. [Hint: Connecting a signal to both inputs of a gate is acceptable.]**
   a. An inverter (Input x and output x')
   b. 2-input AND gate (Inputs: x, y and output F = x and y)
   c. 2-input OR gate (Inputs: x, y and output F = x or y)
   d. Could a, b, and c, be accomplished using only NAND gates: Yes or No?

9. [BB] (50 pts.) Using a Karnaugh map, find both the minimal POS and SOP expression for each of the following functions (both for each).

a. $F = \sum_{ABC}(0,2,4,7)$
b. $G = \prod_{WXYZ}(2,3,7,8,11,12,14,15)$
c. H(w,x,y,z) such that H = 1 for input combinations divisible by 2 or 3 (w,x,y,z=0000 is divisible by 2 and 3).

10. [Practice Only] (0 pts.) Draw the specified implementation schematics.

a. AND-OR implementation for 9a.
b. NOR-NOR implementation for 9b.
c. NAND-NAND implementation for 9c.