

EE 109L Review

Name: Solutions
 Closed Book /

Score: _____

1. Short Answer (16 pts.)

- a. Storing temporary values in (**memory** / **registers**) is preferred due to the (**increased** / **decreased**) access time.
- b. **True** / **False**: A circuit whose VOL value is 1 V can successfully communicate a logic '0' to a circuit whose VIL is 0.5 V?
- c. A family of circuits have IOH=-2 mA, IOL = 1mA, IIH = -0.2 mA and IIL = 0.25 mA. How many other inputs can a single output be successfully wired to ensure operation in any condition? **When outputting logic '1' ten gates (2mA/0.2mA) can be connected but when outputting logic '0' only 4 gates (1mA/0.25mA) can be connected. Thus 4 is the limit.**
- d. The address bus of a new computer is 38-bits wide, approximately how many **bytes** of memory and I/O locations can the computer address? Show any work.

$$2^{38} = 2^8 * 2^{30} = 256 \text{ GB}$$

2. Integer Operations (12 pts). Perform the following hexadecimal operations and state whether OVerflow occurred. *For subtraction, find the complement and add.*

$$\begin{array}{r} \text{a.)} \quad \text{C 5 A 0} \\ \quad \text{- 6 8 B E} \\ \hline \end{array}$$

signed ov: **y** /n

$$\begin{array}{r} \text{C 5 A 0} \\ \text{9 7 4 1} \\ + \quad \quad \quad \underline{\quad 1} \\ \hline \text{5 C E 2} \end{array}$$

unsigned ov: y /**n**

$$\begin{array}{r} \text{b.)} \quad \text{F B 4 B} \\ \quad \text{+ 9 F 3 5} \\ \hline \text{9 A 8 0} \end{array}$$

signed ov: y /**n**

unsigned ov: **y** /n

3. Adders (10 pts.)

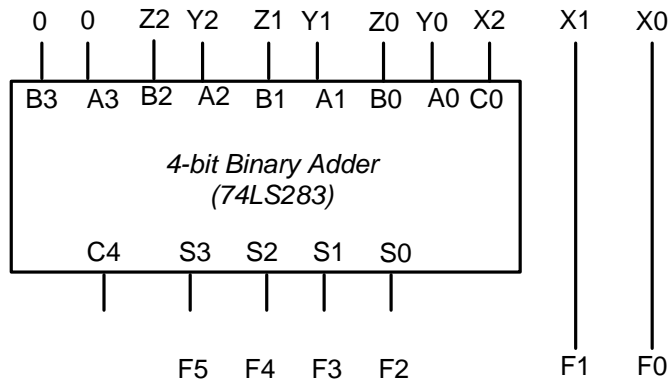
Build a circuit that takes three, 3-bit unsigned numbers, $X[2:0]$, $Y[2:0]$, and $Z[2:0]$, as input and produces an output $F = X + 4Y + 4Z$. **Note:** In binary, multiplying by $4_{10} = 100_2$ simply requires appending two 0's to the end of the number just as in decimal, multiplying by 100 just means adding two 0's (i.e. $937 \cdot 100 = 93700$ in decimal).

a.) How many bits are required for F? (2 pts.)

$$\text{Max} = 7 + 28 + 28 = 63 \Rightarrow 6\text{-bits}$$

b.) The columns of addition are shown below. Implement the addition using a **minimal** number of 74LS283 4-bit adders. One has been drawn below. Add more as necessary. (8 pts.)

			x_2	x_1	x_0
	y_2	y_1	y_0	0	0
+	z_2	z_1	z_0	0	0

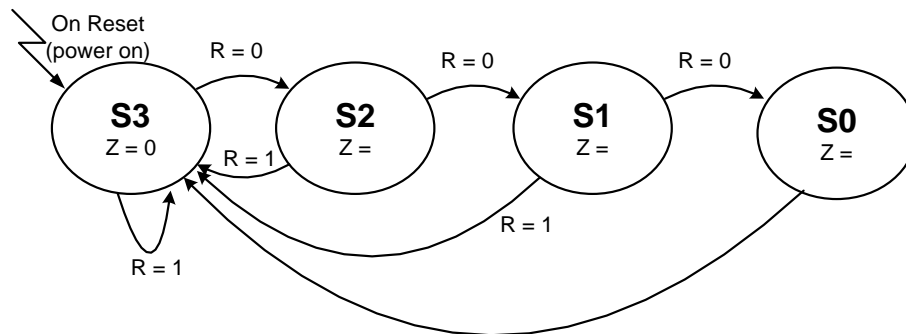


4. **State Machine Design (Down Counter w/ Restart):** Design a synchronous state machine circuit that implements a 2-bit down counter (i.e. counts 11, 10, 01, 00, 11...). The circuit has an external input, R (RESTART), that when '1' should force the counter back to the 11 state no matter what the current state is. As long as R stays '1', the counter should stay in the 11 state. The circuit should also have one output Z. Z=1 when in the 00 state and Z = 0 otherwise.

Let us use 4 states:

S3 (initial state on reset)	The count should be $11_2 = 3_{10}$
S2	The count should be $10_2 = 2_{10}$
S1	The count should be $01_2 = 1_{10}$
S0	The count should be $00_2 = 0_{10}$

- a.) Complete the state diagram below by filling in all necessary transitions **and** the values of Z.



- b.) What is the minimum number of flip-flops required to implement this state machine?

2 Flip Flops

- c.) Complete the state transition/output table given below. (Note: We have provided the state assignment already). We have ordered the states in such a way to use gray code ordering, so take care when translating your state diagram to the transition/output table.

Current State		Next State				Output
State	$Q_1 Q_0$	R=0		R=1		Z
		State	$Q_1^* Q_0^*$	State	$Q_1^* Q_0^*$	
S0	0 0	S3	1 1	S3	1 1	1
S1	0 1	S0	0 0	S3	1 1	0
S3	1 1	S2	1 0	S3	1 1	0
S2	1 0	S1	0 1	S3	1 1	0

d.) Assume we will implement our circuit using D Flip-Flops. Use the K-Maps below to find minimal expressions for D1, D0, and Z.

D₁ Map

		R	
		0	1
Q ₁ Q ₀	00	1	1
	01	0	1
	11	1	1
	10	0	1

$$D_1 = R + Q_1'Q_0' + Q_1Q_0$$

D₀ Map

		R	
		0	1
Q ₁ Q ₀	00	1	1
	01	0	1
	11	0	1
	10	1	1

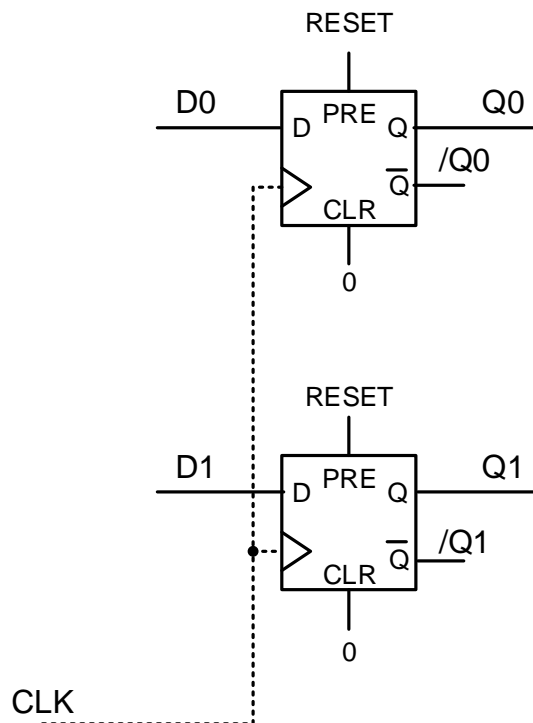
$$D_0 = R + Q_0'$$

Z Map

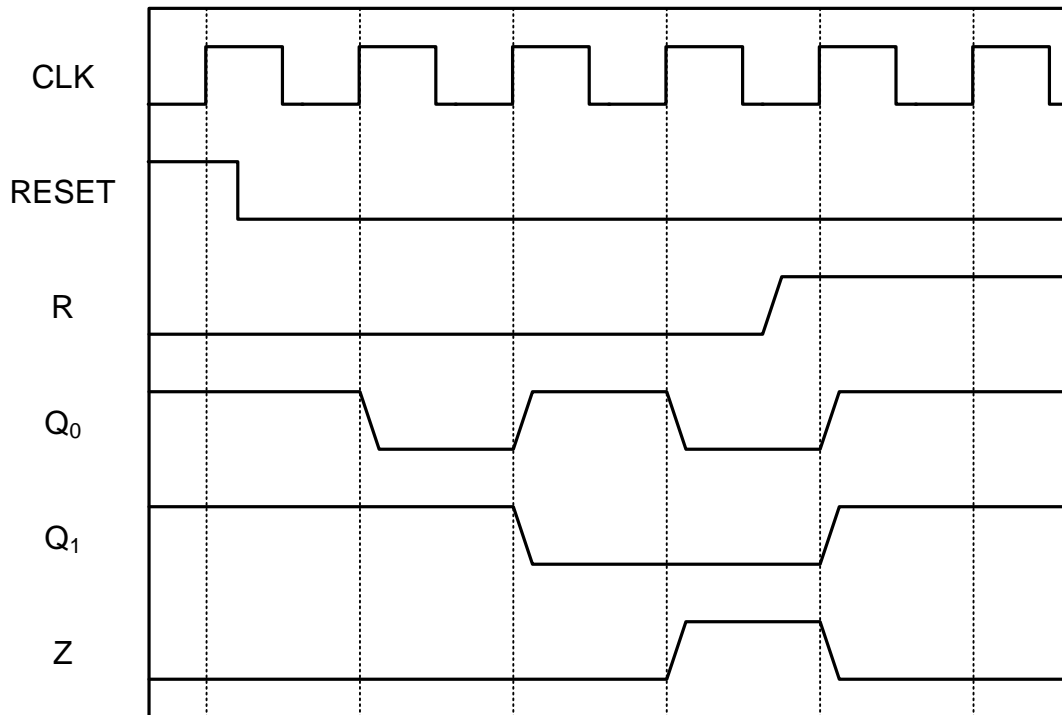
		Q ₁	
		0	1
Q ₀	0	⁰ 1	² 0
	1	¹ 0	³ 0

$$Z = Q_1'Q_0'$$

e.) Show how to implement the initial state (power-on/reset state) by connecting the PRE (PRESET) and CLR inputs of the FF's appropriately. Assume the signal /RESET is available to you. You do not need to implement the next-state or output-function logic.



f.) Using your design above draw the waveform for the sequence of states that the machine will go through and what the output will be for the given input sequence of X. Remember you are using positive edge-triggered devices.



5. True / False

a.) A 4-to-1 multiplexer requires at least 4 select lines: **true / false**

FALSE

b.) 3 separate 2-to-1 muxes can be used to build a single 4-to-1 mux: **true / false**

TRUE

c.) 5 flip-flops are required to implement a state machine with 5 states: **true / false**

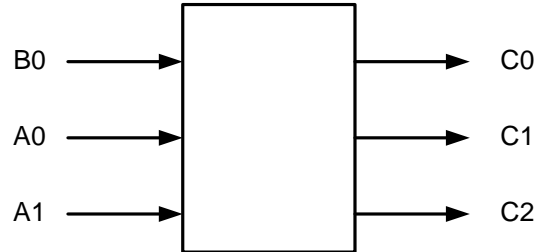
FALSE

d.) In binary, performing $X-Y$ can be performed by adding X to the 2's complement of Y :
true / false

TRUE

6. Design a circuit takes a 2-bit, **unsigned** number $A=(A_1A_0)$ and a 1-bit, **unsigned** number $B=(B_0)$ as input and produces the output $C = A - B$ represented in the 2's complement system. (25 pts.)

- a.) Complete the block diagram of this circuit by showing and labeling the inputs and outputs. Think how many output bits are required. (2 pts.)



- b.) Write out a truth table for this circuit. (8 pts.)

A1	A0	B0	C2	C1	C0
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	0	1	1
1	1	1	0	1	0

- c.) Find the minimal **SOP** expression for each bit of output by using the 3 K-Maps furnished below. Make sure to add the variable labels for the axes of each K-Map and add your gray code. **Clearly indicate** the minimal expressions you find for each output. (12 pts.)

		A_1A_0			
		00	01	11	10
B_0	0	0	0	0	0
	1	1	0	0	0

$$C_2 = A_1'A_0'B_0$$

		A_1A_0			
		00	01	11	10
B_0	0	0	0	1	1
	1	1	0	1	0

$$C_1 = A_1'A_0'B_0 + A_1A_0 + A_1B_0'$$

		A_1A_0			
		00	01	11	10
B_0	0	0	1	1	0
	1	1	0	0	1

$$C_2 = A_0B_0' + A_0'B_0$$