Revised 04/2024

# EE 560 Digital System Design

**Units: 4**
**Summer 2024**
**Lecture: T/Th 1 p.m. – 4:40 p.m.**
**Lab: W: 3 p.m.**
**Location:** : OHE-100C, https://courses.uscden.net/d2l/login and at https://bytes.usc.edu/ee560

## Instructor: Prof. Mark Redekopp

**Office: EEB-222 and occasionally (see course calendar) on Zoom (**https://usc.zoom.us/j/307718126)
**Office Hours: See course webpage.**
**Contact Info:** redekopp@usc.edu (Preferred communication via **Piazza)** Office phone: 213-740-6006

## Teaching Assistant(s):

See website

## Course Description

This is a 4-unit graduate course aimed at electrical engineering and computer engineering graduate students with covering hardware system design and implementation, FPGAs, HDL design, timing, FIFOs, Cache, CAMs, SSRAMs, OoO/multi-threaded CPU design, cache coherency, clock-domain crossing, GPGPU, AXI and PCIe bus protocols. Students will use HDLs to design, analyze, simulate and synthesize hardware components targeted to an FPGA. This course contains many lab projects which require substantial time and effort to complete. Students should have ample availability and desire to invest in the course.

**Prerequisite(s):** EE 457L
**Co-Requisite(s):** None.
**Concurrent Enrollment:** None.
**Recommended Preparation**: Strong background in Verilog and/or VHDL language(s)

## Learning Objectives

1. Gain proficiency in the use of VHDL and Verilog to simulate and synthesize hardware designs
2. Implement designs using synchronous SRAMs
3. Gain proficiency using Questasim simulation and Xilinx synthesis tools
4. Understand the design space and implement the structures necessary for out-of-order processors
5. Implement portions of a fine-grained, multithreaded chip multiprocessor
6. Gain fluency in the PHY and DLL layer implementations of PCIe standard
7. Apply knowledge of GPGPU microarchitecture and SIMT execution to implement small, assembly kernels.

## Course Information

### Course Materials

A set of lecture notes will be made available on the course website at http://bytes.usc.edu/ee560.

### FPGA Board

Students will be issued an FPGA board for use during the course. It must be returned in good working condition at the conclusion of the class.

**Laptop**

It is recommended that students have a Windows (or potentially, Linux) laptop capable of running the Xilinx Vivado and Siemens Questasim tool suite. In lieu of that equipment students must use the Viterbi (remote) desktop interface, though performance may be degraded.

## Technological Proficiency and Hardware/Software Required

Students are expected to have basic proficiency in basic command line usage and use of Xilinx and Questasim tool suite.

## Course Websites

1. **Primary website**: All course assignments, content, office hour information, etc. will be posted at our main website: http://bytes.usc.edu/ee560. This site will contain a link to a shared Google Drive folder where we will post all slides, labs, and homeworks. Please ensure you are able to access it.
2. **Q&A website**: A Q&A and announcement website will be utilized: http://www.piazza.com/. All official announcements regarding assignments, lectures, exams, etc. will be made via Piazza. It is your responsibility to check this site often.
3. **Shared Google Folder**: All slides, HWs, Labs, and other relevant documents will be posted in this folder. We will give access to your @usc.edu account.
4. **Brightspace**: Brightspace will ONLY be used to record grades and, in the event of an emergency, Zoom links will be posted there if class must be conducted online.

## Zoom

For on-campus students, in-person attendance is the only supported option for lecture and lab. **See the attendance policy below**. DEN students may obviously attend remotely via the DEN provided remote lecture format, **but SHOULD attend synchronously**. Lecture and lab recordings will be available via the DEN Brightspace section for all students, and should be used to review and re-watch lecture material to truly understand the content.

## Eligibility

Students with an "A-" grade or above in any of the five courses EE457, EE557, EE577a, EE577b, and EE 533, in recent semesters including the current Spring 2023 semester, are eligible to join EE560. Also, students with two "B+" grades in any two of the same five courses are eligible to join EE560. However, enrollment is often limited so priority may be given to students with the strongest academic record. If a student qualifies through his/her grade in a course other than EE457, he/she is still responsible for the material covered in EE457. Placement exam results are **NOT** considered for this selection. Please do not ask for concession on these requirements. These requirements are essential for your success in the course.

## Required Readings and Supplementary Materials

The following textbooks are **recommended** but not required. We recommend you read the sections listed on the course schedule below for the corresponding week **BEFORE** attending the first lecture of that week.

1. *Online resources provided by the instructor.*

## IT Equipment

**Artix A7 FPGA boards:** Students who registered for the course will be issued a Artix A7 board. On-campus students collect it in their first lab meeting. DEN remote students **will be sent an email or Google Survey link** so that they can provide their home address (with email and phone number) for us to ship a Artix A7 FPGA board to each of them. Board **MUST BE** returned at the end of the semester. Failure to do so will result in payment for the board and/or potential delay in posting of your grade.

**Printing capability**: DEN remote students need to have a laser printer so that they can print their Midterm and Final exams and hand-write them. We have conducted timed-remotely-proctored-closed-book exams in the past, but are investigating proctored exams for remote students. In any case, the student should have access to a printer to print the exam, if necessary. Ability to scan pages with handwritten material to PDF

format may also be required (many apps, such as Adobe Scan, for your phone or tablet exist for this purpose).

## Holidays and Make-up Lecture/Lab

| Dates | Holiday | Makeup Date | Location |
|---|---|---|---|
| M, May 27 | Memorial Day, University Holiday | None (No impact) | N/A |
| W, June 19 | Juneteenth, Non-Instructional Day | M, June 17 | TBA |
| Th-F, July 4-5 | Independence Day | Video Recordings | N/A |

## Description and Assessment of Assignments

### Homeworks

**Availability**: Assignments will be made available on the course shared folder. These assignments are predominantly for your own practice as significant exam material may be drawn from these homeworks. You are strongly encouraged to work on these individually and seek help from a course staff if you struggle to answer the question (as opposed to looking at the solutions or the work of another student). Some homeworks may be posted with solutions and instead of submitting your own solutions, we may simply ask you to acknowledge that you have studied the solutions and understand the relevant approaches and material.

### Labs

**Overview:** Lab assignments are the primary out-of-class work and should challenge you to deepen the concepts learned in lecture. **Significant time must be invested in these lab assignments**. While most labs may be done in teams of two (no threes), some may be individual. Please check the instructions carefully before starting work in teams.

**Assessment**: For each lab, your team must demonstrate working of their lab to the lab TA/Mentor. Both members must be present to receive credit as the TA will ask questions to verify each team member has contributed to your solution. While not on the official schedule, to make efficient use of lab time, we have scheduled an **open lab hours on Fridays, 1:30-3 p.m. for demonstrations**. A room for these hours will be announced as soon as possible.

**Submitting Your Code/Answers**: Code and answers to lab questions (write-ups and/or program source code) must be submitted online (via the USC UNIX/Linux student computing facility**). Instructions for submitting will be provided with the lab and MUST be completed by 11:59 PM Pacific time on the due date.** We will likely have automated scripts that check for and run your code multiple times a day and will email you if your solution does not work. You may then resubmit any number of times.

**Collaboration and Academic Integrity**: Indicated lab assignments are to be completed either individually or in teams of two unless otherwise noted. **NO TEAMS OF 3 or MORE ARE ALLOWED**. **Copying (and then modification) or even LOOKING at or for any portion of code from Internet sources, generative AI sources, fellow, or past students is prohibited** unless cleared with the instructor. We will be clear: **You are not to share or look at the code from another team**. See the Statement on Academic Conduct.

**Late Submission**: No credit will be given for demonstrations or code submissions after the due date(s). **It is your responsibility to submit on time. Don't procrastinate but submit early and often!** No excuses for WiFi connectivity, broken laptops, etc. will be allowed.

**Grading Disputes**: Any disputes with posted grades must be raised within 7 days of the score posting. Notice that any regrade request will result in us trying to give the fairest possible grade to you, which could be higher or lower than the one you received originally. Please see your TA to start the process and hopefully resolve the issue.

**Exams**

**Time and Location**: There will be one midterm. The date of the midterm is shown on the attached schedule but may be moved to a different date in exceptional cases. The exams may also be moved to a different classroom. Always check with the instructor as the listed exam date approaches to confirm the date and time. The exam dates will be announced in class and on the web site. You are responsible for finding out when and where the exams will be held. Makeup exams will be given only for a valid excuse (e.g. serious illness or accident acknowledge through Campus Support (support@usc.edu), urgent family issues, etc., but proof will be required).

**Exam Style**: Exams are designed to not only test your retention of the material but your ability to apply it to design and analyze new or novel problems. In this way, your mastery and depth of understanding of the course content will be assessed. Most questions will come from design problems or applying the skills learned in class. This is where struggling with the homework and lab problems on your own and until you truly understand and feel comfortable with each concept will greatly pay off. *Students who simply "get the lab done" without reviewing and understanding each facet will often struggle on the exam*s. While the instructor may alter the exam medium, it is likely we will use a combination of written (pen/paper) exams and **Gradescope**.

## Attendance Policy

EE560 course runs very fast and we cover substantial amount of material in each lecture and each lab. Ninety percent of the students in EE560 do not require this attendance measure but if it benefits the 10% of the class, we hope the rest of the class does not mind this measure.

| | |
|---|---|
| 1 missed lecture | No penalty |
| 2nd missed lectures | 1% of the course grade |
| 3-4 absences | 2% of the course grade for each such absence |
| 5 or more absences | 3% of the course grade for each such absence |

| | |
|---|---|
| 1 missed lab | No penalty |
| 2nd missed lab | 1% of the course grade |
| 3-4 missed labs | 2% of the course grade for each such absence |
| 5 or more missed labs | 3% of the course grade for each such absence |

Since there are penalties associated with lecture/lab absence, a “a proxy” signature by your friend is considered as cheating, and you and your friend get reported to OAI for an academic integrity violation. So, if you plan to be absent to a lecture or lab, send an email BEFORE the beginning time of that lecture (email the instructor) or lab (email the TA).

## Grading Breakdown

| Assignment | % of Grade |
|---|---|
| Homeworks | 5% |
| Labs | 45% |
| Midterm | 25% |
| Final | 25% |

## Grading Scale

Course final grades will be determined using the following scale. If the grade distribution is lower than expected the scale may be shifted downward but will never be shifted upward.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| A | 94-100 | B+ | 87-89 | C+ | 77-79 | D+ | 67-69 | F | 59 and below |
| A- | 90-93 | B | 83-86 | C | 73-76 | D | 63-66 | | |
| | | B- | 80-82 | C- | 70-72 | D- | 60-62 | | |

## Academic Integrity

The University of Southern California is foremost a learning community committed to fostering successful scholars and researchers dedicated to the pursuit of knowledge and the transmission of ideas. Academic misconduct is in contrast to the university's mission to educate students through a broad array of first-rank academic, professional, and extracurricular programs and includes any act of dishonesty in the submission of academic work (either in draft or final form).

This course will follow the expectations for academic integrity as stated in the USC Student Handbook. All students are expected to submit assignments that are original work and prepared specifically for the course/section in this academic term. You may not submit work written by others or "recycle" work prepared for other courses without obtaining written permission from the instructor(s). Students suspected of engaging in academic misconduct will be reported to the Office of Academic Integrity.

Other violations of academic misconduct include, but are not limited to, cheating, plagiarism, fabrication (e.g., falsifying data), knowingly assisting others in acts of academic dishonesty, and any act that gains or is intended to gain an unfair academic advantage.

We, the EE560 teaching team (instructor, TAs, and graders), wish to differentiate "helping" from "cheating". Students in design classes such as EE560 often need help and sometimes they cannot approach their TAs/instructor. We encourage students to seek help from other students as long as the student offering help acts like a "Teaching Assistant". The student, who is offering help, shall not give away his/her own solution or code or homework as part of the help. The student, who is offering help, shall not try to benefit from looking at the incomplete work of the student, who is receiving help. To the extent possible, actual code/design should not be used in discussing a point. If you are the student who is offering help, think what kind of help the TA or the instructor would offer if the student approached the TA or the instructor instead of approaching you. You can only help him/her to figure out the error in his/her thinking/coding/design without giving away the solution. Often the help may be in debugging. You should not sit down and start writing the code or completing the schematic. You can discuss the various ways to systematically debug and may try to point out the possible errors causing the specific erroneous behavior of the code/design. **If the student seeking help has not done anything towards the assignment and simply comes to you for help, please refuse to help because it is obvious that he/she is looking to receive your work**. Some students procrastinate until the last day and start panicking. There is no way anyone can help such students. We expect that a few students (less than 10% of the EE560 class) fall under this category. Because of these few students, if we prohibit helping all together, we would be doing disservice to the upper 90% of the class.

Once again, in EE560, the students are encouraged to seek help from each other in order to improve their learning of the subject matter and seek help on assignments provided it is purely to clarify a point rather than to share the solution. Observe the same guideline in posting questions and responding to posted questions on the discussion board on the course Blackboard.

Most cheating instances will result in a failing grade F for the course for both students involved in cheating: the student who received unacceptable help and the student who provided unacceptable help. So, we want to warn all students including the "good" students who may think that it is ok for them to give away their design/code because they are not receiving any help.

The impact of academic dishonesty is far-reaching and is considered a serious offense against the university and could result in outcomes such as failure on the assignment, failure in the course, suspension, or even expulsion from the university.

For more information about academic integrity see the student handbook or the Office of Academic Integrity's website, and university policies on Research and Scholarship Misconduct.

**Policy for AI-generated work**
Since creating, analytical, and critical thinking skills are part of the learning outcomes of this course, all assignments should be prepared by the student working according to the policies stated above. Students may not have another person or entity complete any substantive portion of the assignment. Developing strong competencies in these areas will prepare you for a competitive workplace. **Therefore, using AI-generated tools is prohibited in this course (even for small portions), will be identified as plagiarism, and will be reported to the Office of Academic Integrity**.

**Collaboration**. In this class, you are expected to submit work that demonstrates your individual mastery of the course concepts UNLESS team/group work is explicitly designated (i.e. most labs can be done in teams of 2). Unauthorized group work will be considered plagiarism and reported to the Office of Academic Integrity.

**Computer programs**. Plagiarism includes the submission of code written by, or otherwise obtained from someone else.

If found responsible for an academic violation, students may be assigned university outcomes, such as suspension or expulsion from the university, and grade penalties, such as an "F" grade on the assignment, exam, and/or in the course.

## Course Content Distribution and Synchronous Session Recordings Policies

USC has policies that prohibit recording and distribution of any synchronous and asynchronous course content outside of the learning environment.

Recording a university class without the express permission of the instructor and announcement to the class, or unless conducted pursuant to an Office of Student Accessibility Services (OSAS) accommodation. Recording can inhibit free discussion in the future, and thus infringe on the academic freedom of other students as well as the instructor. (Living our Unifying Values: The USC Student Handbook, page 13).

Distribution or use of notes, recordings, exams, or other intellectual property, based on university classes or lectures without the express permission of the instructor for purposes other than individual or group study. This includes but is not limited to providing materials for distribution by services publishing course materials. This restriction on unauthorized use also applies to all information, which had been distributed to students or in any way had been displayed for use in relationship to the class, whether obtained in class, via email, on the internet, or via any other media. (Living our Unifying Values: The USC Student Handbook, page 13).

**Not open to the public**:
The entire content of the course (lectures, labs, slides, video recordings, etc.) is for the registered students of the course only. I request the registered students not to share EE560 course material with anyone (even if the person belongs to USC). We want only the registered students to benefit from this material. We can be a little selfish to maintain the benefits of taking EE 560! 😊

## Course Evaluations

Course evaluation occurs at the end of the semester university-wide. It is an important review of students' experience in the class. The instructor will leave time for you to complete the evaluations (given on Blackboard) during the last week of the course.

## Course Content

**Some topics may be covered through prerecorded lectures**: Since the material is vast, and since we lose some lectures to holidays, we will have to cover a few topics through prerecorded lecture postings.

**Topics of the course**: The EE560 course (Digital System Design course) deals with hardware architecture and implementation of fairly complex hardware systems. It builds upon the pipelined CPU architecture taught in EE457 and tries to teach design detailing and implementation techniques. Too often we come across graduate students who can only talk about hardware design but cannot implement even a simple 5-stage CPU. At USC, we want our students to be able to design and implement (at RTL level) whatever they can architecturally imagine. EE560 tries to achieve this ambitious goal through carefully designed labs and projects. Several DR (Directed Research) students and TAs have worked with Prof. Gandhi Puvvada in the past 25+ years on these EE560 labs/projects.

The major four design and implementation projects are (i) out-of-order instruction-executing CPU (ii) multi-threaded multi-core CPU with cache coherence (iii) PCIe (PCI express) Datalink layer and Physical layer (logical) and (iv) GPGPU (General Purpose Graphical Processing Unit). In Fall 2019 and Spring 2020, a team of 8 DR students and Prof. Puvvada worked on this GPGPU design and implementation project. Much was learned along the way and they were able to incorporate it successfully into EE560 for the first time in Summer 2020.

Besides these, the EE560 covers VHDL, Verilog, FPGA Synthesis, timing design, and several system-design issues. Topics include simple mesh network for processor-memory communication following AXI protocol, FIFOs, Synchronous SRAMs, Synchronous DRAMs, latch-based pipeline with slack borrowing/time stealing, non-linear pipeline design, gated clocking, cache/CAM design, UART, ChipScope (the on-chip logic analyzer), File I/O between the PC and user FPGA board, etc.

The lab/project designs are provided to you in 70% completed form for you (and your teammate) to complete the remaining 30%. However, you need to understand the complete 100% of the design to be successful in the EE560 exam and to able to explain your design to your interviewers. For most of the designs, besides testing and proving them in simulation, you also implement them on a FPGA, and finally test them on the FPGA board (Artix A7 FPGA boards).

**Additional details regarding the four major projects:**

1. **OoO Tomasulo processor**: It executes instructions in out-of-order by dynamically scheduling instructions ready for execution. It performs speculative execution through branch prediction and in-order commitment through a reorder buffer (ROB). It flushes junior instructions in the backend (and in the reorder buffer) in case a branch is found to be mispredicted. It has a Physical Register File (PRF) (not the usual architectural register file), a Free Register List (FRL), a FRAT (Front-end RAT (Register Alias Table)), and a Checkpoint mechanism to quickly recover after a branch misprediction. Physical register Files, Free Register Lists, RATs (Register Alias Tables) and check pointing mechanisms are used in many current processors from Intel and others.

2. **A 4-core processor with each core running 4 thread**s: Cache coherency among the L1 caches in the 4 cores is maintained using MOESI cache coherency protocol. It supports mutual exclusion among the 16 threads via locks in shared memory. MIPs LL (Load-Linked) and SC (Store-Conditional) instructions provide mutual exclusion and synchronization. Non-blocking cache with MSHRs (Miss Status Handling Registers) is implemented to support execution of the remaining active threads while some threads have experienced cache misses.
CPU is tested with example assembly language codes running on the 16 threads and interacting through shared memory locations using two methods (i) with locks and (ii) without locks (lock-free).

**3. PCIe (PCI express):** Students design parts of the Physical Layer (Logical) and Data Link Layer. Students learn LTSSM, 8B/10B encoding and decoding, elastic buffer design, Lane-to-lane de-skewing, Data Link Layer and Ack/Nack protocol. They design parts of the system, integrate the system, and test and understand how to verify critical parts of the design using Chipscope (Xilinx's on-chip logic analyzer) at runtime.

**4. GPGPU**: Our GPGPU implemented on a FPGA supports 8 Warps, each warp consisting of 8 threads. It is a dual issue GPU. It issues and decodes instructions from two warps per cycle. We implemented Scoreboard, SIMT stack, operand collector, banked register file, memory address coalescing, etc. Students are taught the architecture of our design. They write a few assembly language programs to exercise the GPGPU, specifically the SIMT stack.

## Course Schedule

Below is a detailed course calendar —readings, assignments, examinations, etc., broken down on a weekly basis. **As a reminder, for each unit of in-class contact time (i.e. 4 units), the university expects two hours of out of class student work per week over a semester (8 hours).**

| | **Tues. Lecture** | **Wed. Lab** | **Thurs. Lecture** |
|---|---|---|---|
| **Week 1** | | Tools, VHDL, and Vivado<br>Parity Gen., Special Counter, Yards-feet-inches | Course Overview<br>Gated clocking<br>CAM |
| **Week 2** | 5-stage CPU with BRAM | Gray Code Counter,<br>Divider with Cache<br>Chipscope, and UART Assistant | FIFO with BRAM |
| **Week 3** | Clock Skew<br>Timing Analysis<br>Wave Pipelining | CPU with BRAMs<br>(FIFO with BRAMs - tentative) | Tomasulo Part 1<br>Tomasulo Part 2 |
| **Week 4** | Tomasulo Part 3a | Out-of-order Processor – Front-end components | Tomasulo Part 3b |
| **Week 5** | Chip Multiprocessors (CMP) | Out-of-order Processor – Back-end components<br>AXI lab | Chip Multiprocessors (CMP)<br>Barrel shifters / Rotating Prioritizers |
| **Week 6** | PCIe Part 1 | **Mon. 6/17 –** CMP lab<br>Wed. 6/19 – Juneteenth Holiday | PCI Part 2 |
| **Week 7** | GPGPU Part 1<br>Review | **Midterm - June 26 in Lab section** | Lecture: GPGPU<br>**Lab**: PCIe |
| **Week 8** | GPGPU Part3 | PCIe (Synth) – tentative<br>GPGPU (all 3 parts) | **Holiday**<br>(May have recorded lecture if schedule has slipped) |
| **Week 9** | Non-linear Pipelines<br>DRAM, SRAM, DFT | GPGPU<br>Additional Lecture | DRAM, SRAM, DFT |
| | Review or Study day | **Final – July 17 in Lab section** | |

## Statement on Academic Conduct and Support Systems

**Academic Integrity:**
The University of Southern California is a learning community committed to developing successful scholars and researchers dedicated to the pursuit of knowledge and the dissemination of ideas. Academic misconduct, which includes any act of dishonesty in the production or submission of academic work, compromises the integrity of the person who commits the act and can impugn the perceived integrity of the entire university community. It stands in opposition to the university's mission to research, educate, and contribute productively to our community and the world.

All students are expected to submit assignments that represent their own original work, and that have been prepared specifically for the course or section for which they have been submitted. You may not submit work written by others or "recycle" work prepared for other courses without obtaining written permission from the instructor(s).

Other violations of academic integrity include, but are not limited to, cheating, plagiarism, fabrication (e.g., falsifying data), collusion, knowingly assisting others in acts of academic dishonesty, and any act that gains or is intended to gain an unfair academic advantage.

The impact of academic dishonesty is far-reaching and is considered a serious offense against the university. All incidences of academic misconduct will be reported to the Office of Academic Integrity and could result in outcomes such as failure on the assignment, failure in the course, suspension, or even expulsion from the university.

For more information about academic integrity see the student handbook or the Office of Academic Integrity's website, and university policies on Research and Scholarship Misconduct.

Please ask your instructor if you are unsure what constitutes unauthorized assistance on an exam or assignment, or what information requires citation and/or attribution.

**Students and Disability Accommodations:**

USC welcomes students with disabilities into all of the University's educational programs. The Office of Student Accessibility Services (OSAS) is responsible for the determination of appropriate accommodations for students who encounter disability-related barriers. Once a student has completed the OSAS process (registration, initial appointment, and submitted documentation) and accommodations are determined to be reasonable and appropriate, a Letter of Accommodation (LOA) will be available to generate for each course. The LOA must be given to each course instructor by the student and followed up with a discussion. This should be done as early in the semester as possible as accommodations are not retroactive. More information can be found at osas.usc.edu. You may contact OSAS at (213) 740-0776 or via email at osasfrontdesk@usc.edu.

**Support Systems:**

*Counseling and Mental Health - (213) 740-9355 – 24/7 on call*
Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

*988 Suicide and Crisis Lifeline - 988 for both calls and text messages – 24/7 on call*
The 988 Suicide and Crisis Lifeline (formerly known as the National Suicide Prevention Lifeline) provides free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week, across the United States. The Lifeline is comprised of a national network of over 200 local crisis centers, combining custom local care and resources with national standards and best practices. The new, shorter phone number makes it easier for people to remember and access mental health crisis services

(though the previous 1 (800) 273-8255 number will continue to function indefinitely) and represents a continued commitment to those in crisis.

*Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-9355(WELL) – 24/7 on call*
Free and confidential therapy services, workshops, and training for situations related to gender- and power-based harm (including sexual assault, intimate partner violence, and stalking).

*Office for Equity, Equal Opportunity, and Title IX (EEO-TIX) - (213) 740-5086*
Information about how to get help or help someone affected by harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants.

*Reporting Incidents of Bias or Harassment - (213) 740-5086 or (213) 821-8298*
Avenue to report incidents of bias, hate crimes, and microaggressions to the Office for Equity, Equal Opportunity, and Title for appropriate investigation, supportive measures, and response.

*The Office of Student Accessibility Services (OSAS) - (213) 740-0776*
OSAS ensures equal access for students with disabilities through providing academic accommodations and auxiliary aids in accordance with federal laws and university policy.

*USC Campus Support and Intervention - (213) 740-0411*
Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

*Diversity, Equity and Inclusion - (213) 740-2101*
Information on events, programs and training, the Provost's Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

*USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call*
Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

*USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-1200 – 24/7 on call*
Non-emergency assistance or information.

*Office of the Ombuds - (213) 821-9556 (UPC) / (323-442-0382 (HSC)*
A safe and confidential place to share your USC-related issues with a University Ombuds who will work with you to explore options or paths to manage your concern.

*Occupational Therapy Faculty Practice - (323) 442-2850 or* otfp@med.usc.edu
Services for USC students to support health promoting habits and routines that enhance quality of life and academic performance.