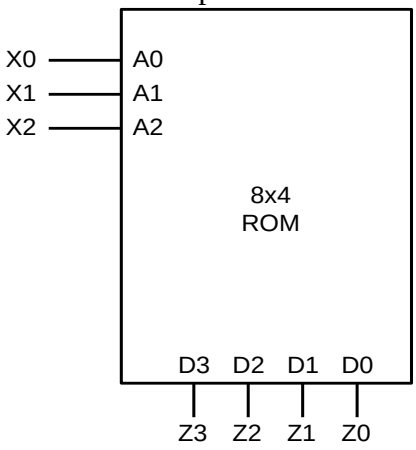
EE 109 Homework 8
FPGAs, ASICs, Memories, & Interfacing

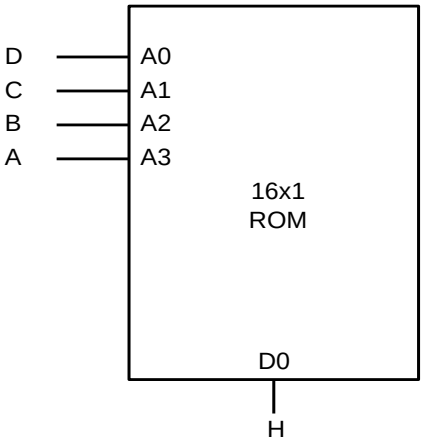
Name: ___Solutions_____
Due: **Score: _____**

1. For each of the following functions list the size of ROM required to implement it (e.g. 256x4 or 8x1). Then, draw the block diagram of the ROM showing the device labels: A[n-1] to A[0] and your data outputs as D[m-1] to D[0] [device labels are inside the block used to indicate which input/output is which] label the address inputs]. Next add appropriate system labels (actual function input and output signals). You need not show the contents of the ROM, just the size.
   a. A circuit that converts a 3-bit 2's comp. number X[2:0] to the equivalent 4-bit signed magnitude number, Y[3:0].
   b. H = Σ ABCD(2,5,6,7,8,10,13,15)
   c. A circuit that takes a 6-bit 2's comp. number, A[5:0], and squares it (B = A2) where B is output in unsigned representation (i.e. squaring always yields a positive result.)

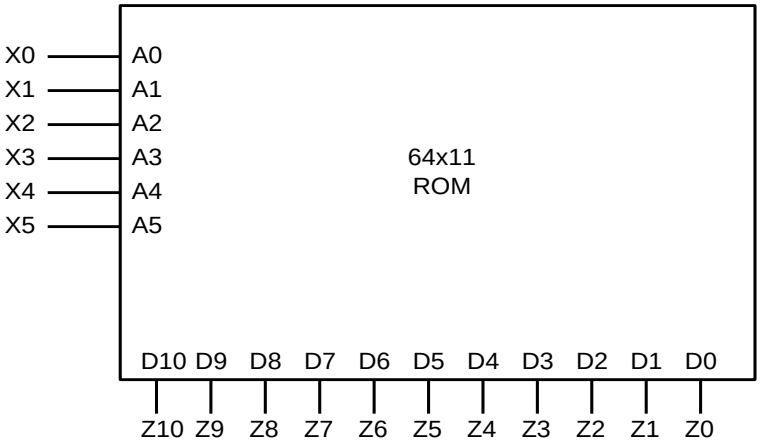
a. – 3-bit inputs = 2^3 rows and 4 outputs



b. – 4-bit inputs = 2^4 rows and 1 output



c. – 6-bit inputs = 2^6 rows and range of 6-bit 2's comp. input is [-32 to +31]. Thus, max ouput is $-32^2 = 1024 = 11$ bits of output



2. Answer the questions below.

	V_{OH}	V_{OL}	V_{IH}	V_{IL}
Family 1	4.0 V	1.0 V	3.2 V	1.3 V
Family 2	4.1 V	0.3 V	3.7 V	0.5 V

a. Given two families of logic with the given voltage levels, list the noise margins: NM_H and NM_L for Family 1.
NMh = |Voh – Vih| = 0.8V
NMl = |Vol – Vil| = 0.3V

b. **True/False**: A Family 2 device outputting to a Family 1 input may fail when outputting HIGH (digital 1)?

FALSE, Family 2 Voh = 4.1V which must be greater than Family 1 Vih of 3.2V to work. And this is satisfied.

c. **True/False**: A Family 1 device outputting to a Family 2 input may fail when outputting LOW (digital 0)?

TRUE, Family 1 Vol = 1.0V which must be lower than Family 2 Vil of 0.5V to work. And this is NOT satisfied.

	$\|I_{OH}\|$	$\|I_{OL}\|$	$\|I_{IH}\|$	$\|I_{IL}\|$
Family 1	600 μA	5 mA	60 μA	1 mA

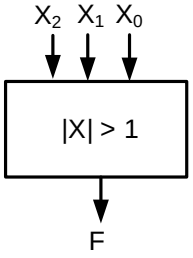
d. What is the maximum fan-out of gates from Family 1 (to other Family 1 gates)?

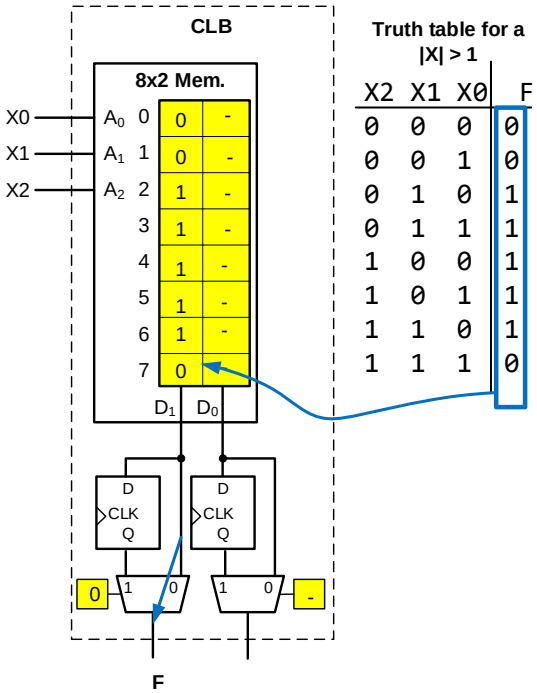
Ratio |Ioh|/|Iih| = 600 / 60 = 10
Ratio |Iol|/|Iil| = 5 / 1 = 5

Maximum fanout = min(|Ioh|/|Iih|, |Iol|/|Iil|) = min(10, 5) = 5
.

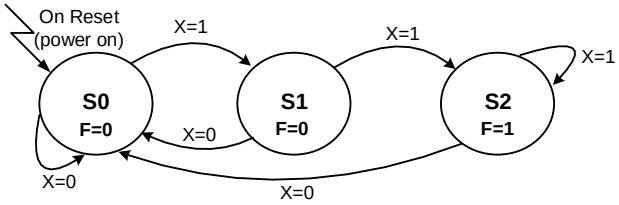
3. Implement the following designs using FPGA-style CLB(s) [Configurable Logic Blocks].
   a. Consider the design of a circuit to detect if the absolute value of a 3-bit 2's complement system number, X, is greater than 1. Rather than building it directly with gates, show how to program a CLB to produce the output by filling in the yellow/highlighted boxes. Hint: Any combinational design can be described with a truth table.

Desired logic circuit:



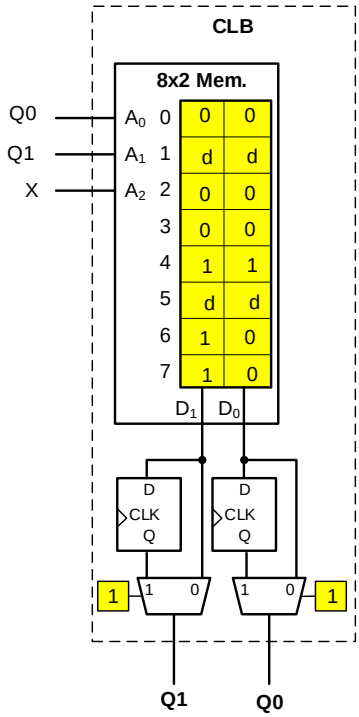


b. Consider the design of the "2-consecutive 1's" sequence detector specified in the State Machines Unit slides and reprinted below:



Current State			Next State						Output
			X = 0			X = 1			
State	Q_1	Q_0	State	Q1*	Q0*	State	Q1*	Q0*	F
S0	0	0	S0	0	0	S1	1	1	0
--	0	1	--	d	d	--	d	d	d
S1	1	1	S0	0	0	S2	1	0	0
S2	1	0	S0	0	0	S2	1	0	1

Given the CLB below, implement the state machine (by filling in the yellow/highlighted boxes) EXCEPT for the output F. That is, implement the next state logic and state memory. Assume the flip-flop outputs (Q1Q0) are fed back to the inputs of the CLB.



4. Matching.

Terms	Descriptions
a.) FPGA = 1 b.) ASIC = 5, 6 c.) SoC = 4 d.) HDL = 2, 3, 8 e.) Synthesis = 9 f.) IP Core = 7, 10	1. Primary product of the companies named Xilinx and Altera (now part of Intel) 2. An example is Verilog 3. An example is SystemC 4. IC that combines processor, memory, and custom digital or analog circuitry 5. A chip that performs a dedicated task 6. Usually faster alternative to an FPGA 7. Circuit or data that is designed/produced by a 3rd party and can be included into a product 8. Common means of describing a digital design that can be used by CAD tools to build an ASIC or FPGA 9. Process implemented by CAD tools of converting a description of a digital device to the physical gates and their interconnection to form an ASIC or FPGA 10. An example might be the hardware design of a JPEG image decoder that can be purchased for use in a larger hardware design.