CS 356 Cache Exercises
Redekopp

Name: _____

Score: _____

Enter answers on Blackboard

1.) (18 pts.) A processor has a 32-bit memory address space (i.e. 32-bit addresses). The memory is broken into blocks of 32 **bytes** each. The computer also has a cache capable of storing 16K **bytes**.
   - a.) How many blocks can the cache store?
   - b.) Assuming the cache uses **direct-mapping**, break the address into TAG, BLOCK, and BYTE OFFSET fields (show which address bits correspond to which field). Show your calculations.

Tag	Block	Byte Offset

   - c.) Assuming the cache uses a **4-way set-associative mapping**, break the address into TAG, BLOCK, and WORD fields (show which address bits correspond to which field). Show your calculations.

Tag	Set	Byte Offset

2.) (18 pts.) A processor has a 36-bit memory address space (i.e. 36-bit addresses). The memory is broken into blocks of 64 **bytes** each. The computer also has a cache capable of storing **1 Megabyte**.
   - a.) How many blocks can the cache store?
   - b.) Assuming the cache uses **direct-mapping**, break the address into TAG, BLOCK, and BYTE OFFSET fields (show which address bits correspond to which field). Show your calculations.
   - c.) Assuming the cache uses a **8-way set-associative mapping**, break the address into TAG, BLOCK, and BYTE OFFSET fields (show which address bits correspond to which field). Show your calculations.

3.) (20 pts.) Exercises 5.3.3 in CO&D, 4th Ed. page 550. You are asked to optimize a cache capable of storing 8 bytes total for the given references. There are three **direct-mapped** cache designs possible by varying the block size: C1 has one-byte blocks, C2 has two-byte blocks, and C3 has four-byte blocks. In terms of miss rate, which cache design is best? If the miss stall time is 25 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design? (Every access, hit or miss, requires an access to the cache)

Do this exercise only for access pattern a below. To make this easier for you, the address sequence has been converted to binary below. First do the address bit breakdown, then complete the table to answer the question.

Address Sequence	LS 8-bits of address	C1 Block Answer [0-7]	H/M	C2 Block Answer [0-3]	H/M	C3 Block Answer [0-1]	H/M
1	0000 0001						
134	1000 0110						
212	1101 0100						
1	0000 0001						
135	1000 0111						
213	1101 0101						
162	1010 0010						
161	1010 0001						
2	0000 0010						
44	0010 1100						
41	0010 1001						
221	1101 1101						
Miss Rate			____/12		____/12		___/12
Time		2*12 + _____ = _____		3*12+____ = _____		5*12+____ = _____	

4.) (20 pts.) Exercises 5.3.5 in CO&D, 4th Ed. page 551. Consider a direct-mapped cache of 64 KB and a block size of 8 bytes. Generate a series of read requests (address sequence) that will have a lower miss rate on a 2 KB 2-way set associative cache with the same block size than this 64 KB direct mapped cache? Then generate a series of read requests (address sequence) that will have a lower miss rate in the 64KB direct-mapped cache. To make answers more standard, use address that are as small as possible to make your case (i.e. make unneeded tag bits of your address 0 [you should just need to change a few of the LS tag bits] and make the byte offset portion [i.e. LSBs] 0 wherever possible).

First do the address breakdown for each cache:

Cache	Tag (A19-A?)	Block or Set	Byte Offset
64 KB, direct, 2 w/block			
2 KB, 2-way SA, 2 w/block			

For the first question, find a 3 address sequence. Write out your address to **20-bits**. (i.e. 0x00800)

	20-bit address in hex.
1	
2	
3	

For the second question, find a 4 address sequence. Write out your address to **20-bits**. (i.e. 0x00800)

	20-bit address in hex.
1	
2	
3	
4	